USING COMPLEMENTARY SILICON-GERMANIUM TRANSISTORS FOR DESIGN OF HIGH-PERFORMANCE RF FRONT-ENDS

A Dissertation
Presented to
The Academic Faculty

by

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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
August 2012

USING COMPLEMENTARY SILICON-GERMANIUM TRANSISTORS FOR DESIGN OF HIGH-PERFORMANCE RF FRONT-ENDS

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To P.G. Wodehouse, Roald Dahl, and Bill Watterson

For making me love the written word.

ACKNOWLEDGEMENTS

"He's only a research professor, he can't teach". "He's only a teaching professor; he has never opened a journal". "He's a good manager, but not very adept technically." Fortunately, it became very clear to me early on that I would never have to traverse these conventional circles of mutual exclusivities under the mentoring of my advisor, Dr. John D. Cressler. He does justice to all roles with élan. His passion for teaching and research inspires me, and it is my honor and pleasure to have worked under his tutelage.

I would like to thank Dr. Shyh-Chiang Shen, Dr. John Papapolymerou, Dr. David C. Keezer, and Dr. Paul A Kohl for serving on my dissertation committee. Their thoughtful inputs throughout this process have served to greatly improve the quality and relevance of this work.

I would like to acknowledge all fellow graduate students in the GT SiGe Research Team for their assistance, for initiating insightful debates that helped to answer numerous questions, and for their companionship. Extra thanks to John Poh, Tushar Thrivikraman, and Rajan Arora.

I would like to express my sincerest gratitude to my parents, Anita and Umesh, in-laws, Deepa and Sudhir, and sister, Swati, for being supportive of me continuously during good and bad times. Lastly, not even a single word of this entire dissertation would have been possible had it not been for the unwavering support of the love of my life – Manasi. We've come a long way from being the teenage lovers that we once were, but my feelings about us haven't changed by even an iota. To Manasi, I owe my doctorate degree.

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SUMMARY

The objective of the research presented in this dissertation is to explore the achievable dynamic range limits in high-performance RF front-ends designed using SiGe HBTs, with a focus on complementary (*npn* + *pnp*) SiGe technologies. The performance requirements of RF front-ends are high gain, high linearity, low *dc* power consumption, very low noise figure, and compactness. The research presented in this dissertation shows that all of these requirements can easily be met by using complementary SiGe HBTs. Thus, a strong case is made in favor of using SiGe technologies for designing high dynamic range RF front-ends. The contributions from this research are summarized as follows:

1. The first-ever comparison study and comprehensive analysis of small-signal linearity (IIP3) for *npn* and *pnp* SiGe HBTs on SOI [1].
2. A novel comparison of large-signal robustness of *npn* and *pnp* SiGe HBTs for use in high-performance RF front-ends [2].
3. A systematic and rigorous comparison of SiGe HBT compact models for high-fidelity distortion modeling [3].
4. The first-ever feasibility study of using weakly-saturated SiGe HBTs for use in severely power constrained RF front-ends [4].
5. A novel X-band Low Noise Amplifier (LNA) using weakly-saturated SiGe HBTs [5].
6. Design and comprehensive analysis of RF switches with enhanced large-signal linearity [6].

7. Development of novel methods to reduce crosstalk noise in mixed-signal circuits and the first-ever analysis of crosstalk noise across temperature [7].
8. Design of a very high-linearity cellular band quadrature modulator for use in base-station applications using first-generation complementary SiGe HBTs.

CHAPTER I

INTRODUCTION

1.1 Microtechnology: A Macro View

World War II had just ended; the twin marvels of the Manhattan Project, Little Boy and Fat Man, delivering what they had promised – a liberated world enabled by America's military might and scientific prowess [8]. Buoyed by this success, a proposal to "institutionalize" scientific research submitted by Vannevar Bush to the President was being given serious consideration in Washington policy circles [9]. All over the country, even as US infantry was making its way back to the homeland after prolonged skirmishes aboard, civilian life had returned back to normal.

Around this time, John Bardeen, a scientist who worked at the Naval Ordnance Laboratory during the war, was seeking a return to academia at the University of Minnesota (UMN). He had turned down an invitation to join the Manhattan Project two years ago [10]. His area of expertise – theoretical solid-state physics – was a very nascent field of science which did not interest UMN very much. Interested in Bardeen's work, however, were scientists at Bell Labs in Murray Hill, New Jersey, who had only recently started work on applied solid-state physics. As soon as he was made a competitive offer by Bell Labs, Bardeen was quick to abandon his academic career in favor of an industrial one. At Bell Labs he would work under the supervision of William Shockley, whom Bardeen had met while going to school in Massachusetts. He would also work alongside an experimentalist by the name of Walter Brattain, a friend of Bardeen's from graduate school in Princeton. The roles within the trio of Shockley, Bardeen, and Brattain were well established. Shockley would come up with an idea, Brattain would work hard to implement Shockley's idea in the lab, and Bardeen would come in later and try to wrap theory around why Shockley's idea did or did not work, thus completing the feedback loop.

Figure 1: From left to right: John Bardeen, William Shockley, and Walter Brattain. Image courtesy of AT&T archives and Wikimedia Commons.

In early 1947, the trio was working to identify why a thought experiment of Shockley's (a non vacuum-tube amplifier) would not work in the lab. During the summer of 1947, Bardeen worked tirelessly to correct the theory behind a device that could enable Shockley's envisioned amplification. Merely two days before Christmas, while all the lab personnel (including Shockley) were on vacation, Bardeen and Brattain observed that their point-contact device, a germanium crystal connected to external voltage-sources using gold foil as ohmic contacts, was showing signs of amplification. This point contact-transistor, also shown in Figure 2, achieved the same amplification results as a vacuum-tube, while being only $1/50^{th}$ of the tube's size, thereby enabling extreme miniaturization of all existing electronics. Thus on December 23^{rd}, 1947, the world's first ever solid-state amplifier was brought into existence. All electrical engineers today can trace back their trade to that single date in history! The invention of the transistor earned Bardeen, Shockley and Brattain a Nobel Prize in Physics in 1956.

Figure 2: The first ever point-contact transistor, made from Germanium crystal and gold foil contacts. Image courtesy of Alcatel Lucent/Bell Labs.

That point-contact transistor from 1956 (shown in Figure 2) was, in both operation and design, the grandfather of the modern-day Silicon-Germanium Heterojunction Bipolar Transistor (HBT).

1.2 SiGe HBT BiCMOS Technology

For the past decade or so, Silicon-Germanium (SiGe) bipolar complementary metal-oxide semiconductor (BiCMOS) technology platforms have been receiving increased interest in the radio-frequency (RF) circuit design community. It is not hard to fathom why – SiGe based circuits and systems now achieve similar performance as their III-V counterparts (gallium-arsenide and gallium-nitride based circuits), while maintaining the low-cost advantages of complementary metal oxide semiconductor (CMOS) technologies. The interest of the RF design community in SiGe has sustained due to its improving performance metrics over the years. With a peak unity gain frequency (f_T) and maximum oscillation frequency (f_{MAX}) approaching 500 GHz (as

shown in Figure 3), SiGe HBTs are ideal for use in high-performance circuits such as RF low-noise amplifiers (LNA), power amplifiers (PA), and other sub-circuits in the transmit-receive (TR) chain such as mixers, voltage controlled oscillators (VCO) etc [11, 12]. With a rapidly increasing consumer base in RF technologies, using low-cost high-performance SiGe platforms to design RF chips is very profitable. For that reason, it becomes imperative for us to study SiGe technologies, with an emphasis on device metrics that directly translate into highly aggressive RF circuits, such as in [13].

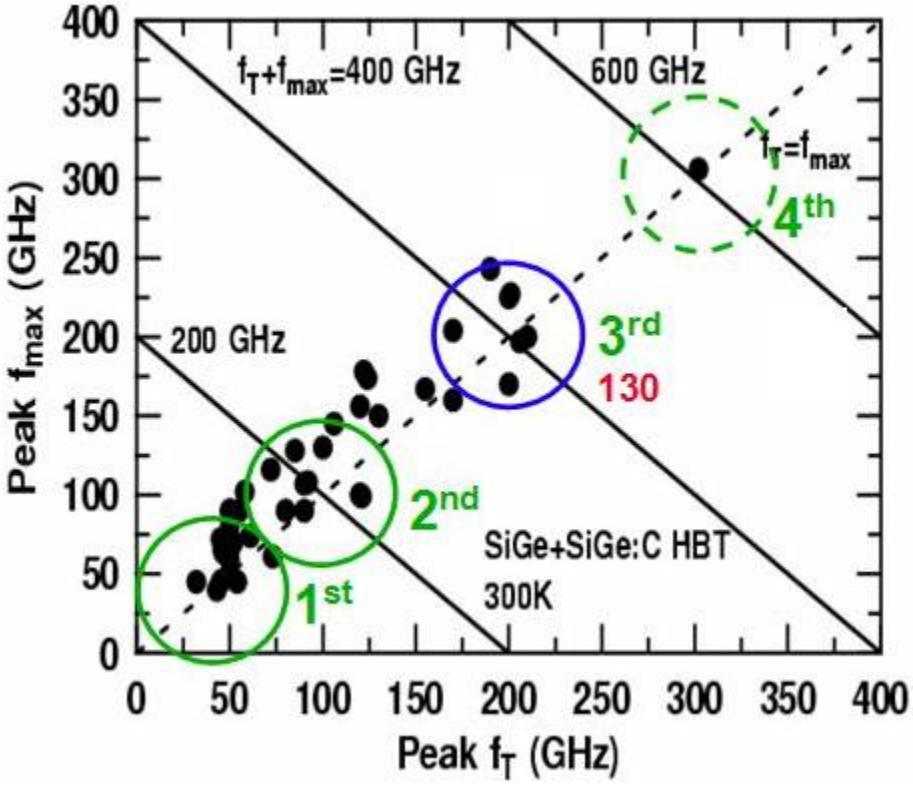

Figure 3: The evolution of f_T and f_{MAX} for SiGe HBTs across many generations [11].

The enabler of these aggressive performance metrics in SiGe platforms has been the incorporation of germanium in the base of a standard silicon (Si) bipolar junction transistor (BJT). Enabled by band-gap engineering, SiGe platforms enjoy improvements in performance metrics such as current gain (β), Early voltage (V_A) and f_T over their standard Si BJT counterparts [11]. The ease of integration of germanium in the base of standard Si BJT processes permits superior levels of system complexity, while leveraging

the benefits of the best-of-breed Si CMOS technologies for potent use in mixed-signal application domains.

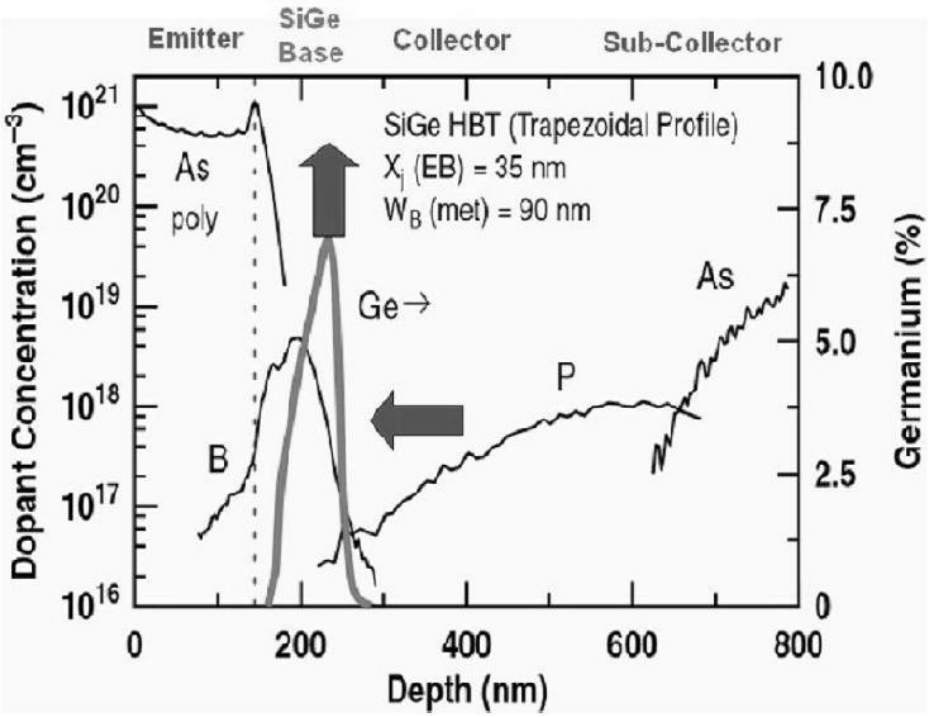

Figure 4: Vertical doping profile showing doping concentrations and Ge profile inside a first-generation SiGe HBT [11].

As mentioned previously, a key difference between a Si BJT and a SiGe HBT is the inclusion of graded germanium in the active base region of the Si BJT. In *npn* HBTs, this is enabled by adding a layer of compositionally graded SiGe alloy in the boron-doped epitaxial layer. Figure 4 shows the doping profile for a first-generation SiGe HBT. The germanium layer is usually grown epitaxially using ultra-high vacuum/chemical vapor deposition (UHV/CVD) techniques discussed in [14]. This step is an easy add-on to the standard Si CMOS process flow, and does not affect the HBT performance, the CMOS yield and overall throughput [11]. It also does not disturb the overall thermal budget of the fabrication process. The epitaxial layer is the enabler of band-gap engineering, which leads to high-performance devices while still maintaining process compatibility with standard Si CMOS manufacturing.

More than four generations of SiGe HBTs exist in production (Figure 3). They are used in a host of application such as cellular phones, wireless telemetry, radar systems, and satellite communications. The transistors used in this work are the third-generation *npn* SiGe HBTs from IBM [15], complementary SiGe HBTs on thick-film SOI from National Semiconductor (NSC) [16], as well as first-generation complementary SiGe HBTs from Texas Instruments (hitherto unpublished, similar to the HBTs in [17]).

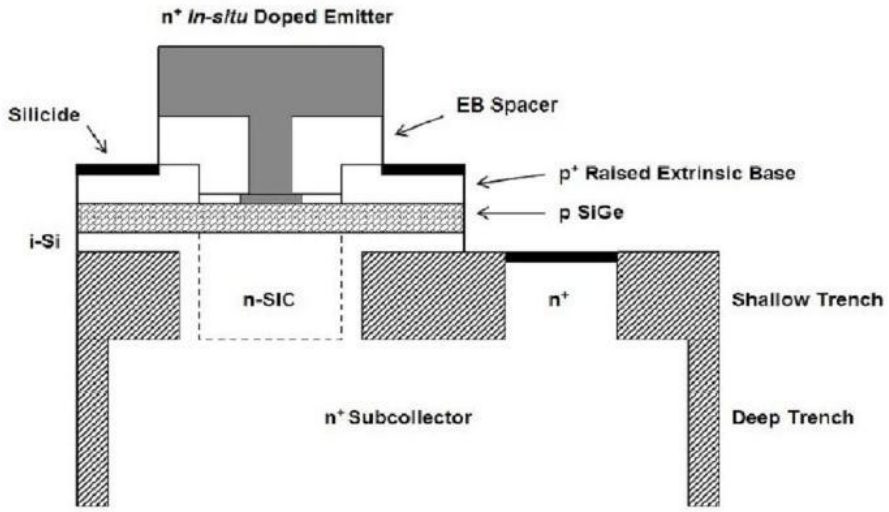

Figure 5: A schematic cross section of a third-generation BiCMOS SiGe HBT [12].

A cross-section of a third-generation device from IBM [15] is shown Figure 5. Due to a number of advantages, a vertical self-aligned scheme is used. The main advantage of using this scheme is the reduction in internal transistor parasitics, which is responsible for giving the transistor aggressive f_{MAX} metrics, as well as reduced low-frequency 1/f noise due to mitigated surface effects. A thin base region translates directly into a faster transit time for the electron (from emitter to collector), lending itself to a faster f_T metric [12]. To prevent the base region from diffusing out and thus compromising its thinness, it becomes important to employ a UHV/CVD epitaxial

fabrication step that does not tax the thermal budget of the process flow too much [18]. Carbon is used in addition to boron to prevent the out-diffusion of the base in other process steps [19]. Thus, with UHV/CVD and carbon in base, a narrow base profile is maintained. The technology also incorporates deep-trench isolation (DTI) and shallow-trench isolation (STI). A selectively-implanted collector (SIC) enables IBM to manufacture the HBTs with varying speeds and breakdowns.

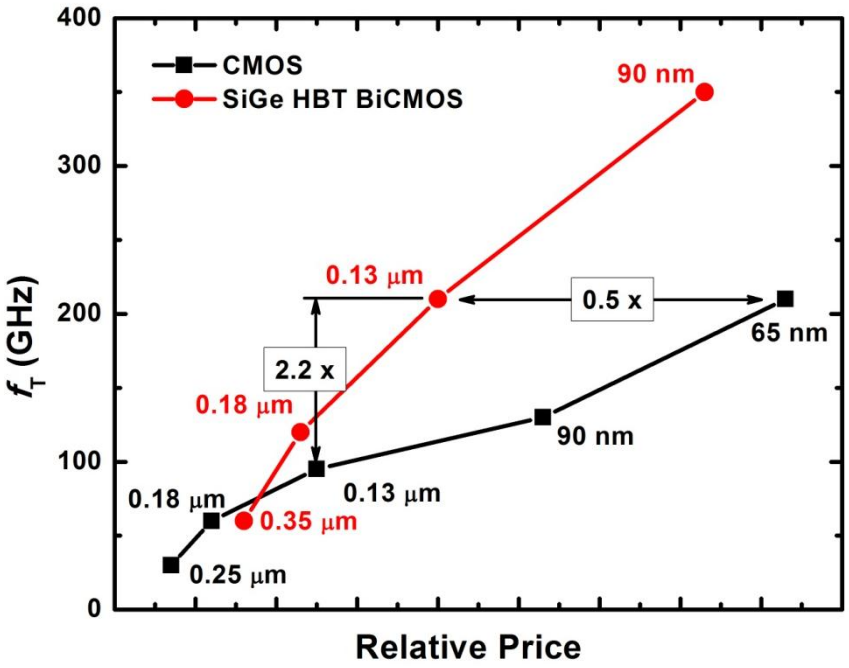

Figure 6: Price-performance comparison between SiGe HBT BiCMOS and CMOS technologies.

As a last note, it may be argued that highly-scaled CMOS transistors are now able to achieve the same level of performance as SiGe HBTs, with the added advantage of higher integration with digital blocks. While this is true, it can be seen from Figure 6 (from [20]) that to achieve f_T performance of, say, 200 GHz, the 65-nm CMOS technology which is able to support such fast speeds costs twice as much as the equally fast 0.13-μm SiGe process. Evaluated at the same scaling node (e.g. 0.13-μm), the performance of SiGe HBTs is better than a comparably scaled CMOS FET by more than

a factor of two. Thus SiGe technologies truly enable III-V like performance at the price of vanilla CMOS manufacturing!

1.3 Introduction to Distortion

SiGe technologies have found widespread uses in wireless local area networks (LAN), cellular telephony, and satellite systems. Unlike wired communication, these types of communications all rely on a common transmission medium. Unfortunately, the available spectrum is limited and interference with other transmission media has to be avoided at all costs. Various transistor, circuit, and system level techniques have to be applied to ensure adequate circuit performance within the limited spectrum allotted for its operation [21].

Keeping the above constraints in mind, it becomes important for T/R systems to utilize the frequency spectrum allotted to them efficiently without causing interference. In addition, such systems should be able to work with signals ranging from very weak to very strong without loss of signal integrity.

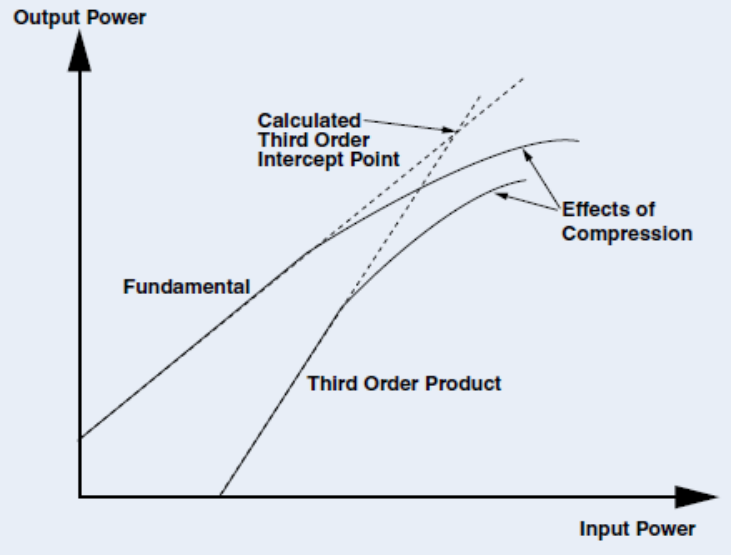

Figure 7: Small-signal and large-signal nonlinearities in an amplifier.

For a T/R system to meet these stringent demands is not easy. As shown in Figure 7, a major source of distortion in any circuit with active amplifying devices (such as HBTs, FETs) is known as “Gain Compression”. When an incoming RF signal, by virtue of its large magnitude, is able to influence the quiescent *dc* bias operating-point of an amplifier, it leads to distorted waveforms at the output. In such cases, the output RF signal does not amplify linearly as a function of the input RF signal. Gain-compression is an example of “large-signal” nonlinearity, and is described in detail in Section 1.3.1.

Another instance of nonlinearity arises when two closely-spaced frequencies are present at the input of an amplifier. This happens very frequently in commercial applications such as audio amplifiers, Global Positioning Systems (GPS), and cell phone receivers. Such an amplifier has a tendency to generate spurious frequencies (third-order and fifth-order products) at its output that can interfere with adjacent frequency bands in a tightly crowded spectrum. This phenomenon is called “Intermodulation Distortion” and is quantified by a metric known as “Third-Order Intercept Point” (IP3). Intermodulation Distortion is described in detail in Section 1.3.2.

Thus, in summary, there are two types of non-linearities in active circuits - “Gain Compression”, and “Intermodulation Distortion”. They are discussed one by one. It should be pointed out that the terms “nonlinearity” and “distortion” mean the same thing, and will be interchangeably used within this dissertation. Both terms signify the same phenomenon, that of RF circuits or systems not generating outputs linearly with increasing input signal levels.

1.3.1 Gain Compression

Assume an amplifier has a single excitation frequency ω_1 at its input. The output of the amplifier should contain the same frequency ω_1 but magnified in its signal amplitude. In an ideal amplifier, the input *x(t)* and output *y(t)* should follow the relationship:

$$y(t) = k_1 x(t). \tag{1}$$

Here k_1 is equal to the gain of the amplifier. Due to inherent non-linearities in the amplifier, however, the input-output relation is governed by the following power-series expansion:

$$y(t) = k_1 x(t) + k_2 x^2(t) + k_3 x^3(t) + \cdots. \tag{2}$$

As a result, for an input $x(t) = A\cos(\omega_1 t)$, the output takes the shape:

$$y(t) = \frac{k_2 A^2}{2} \qquad (DC\ shift)$$

$$+\left(k_1 A + \frac{3k_3 A^3}{4}\right)\cos\omega t \qquad (Fundamental\ Tone)$$

$$+\frac{k_2 A^2}{2}\cos\omega t \qquad (Second\ Harmonic)$$

$$+ \ldots \quad . \tag{3}$$

Thus, in addition to the amplified input frequency generated at the output, additional tones such as higher order harmonics are present, accompanied by a DC offset term. The gain of this amplifier is not merely "k_1" anymore, but a complex term including third-order expansion terms denoted by

$$k_1 A + \frac{3k_3 A^3}{4}.$$

For a small input signal magnitude A, the second term of the fundamental tone in the output expression (equation 3) can be neglected. However with increasing input signal magnitude A, $3k_3A^3/4$ becomes equal to, and then larger than, the actual output magnitude k_1A. Usually $k_3<0$, which translates into diminishing gain values at sufficiently

high input signal magnitudes *A* in an amplifier. The gain thus "compresses" with increasing input signal magnitudes. This is a fundamental manifestation of nonlinearity. It leads to a degraded signal-to-noise ratio (SNR) in RF circuits, as well as degradation in bit error rates (BER) performance of digital circuits. The input signal power level that induces gain compression is quantified by the term "1-dB Compression Point", or "P1dB". For a "P1dB" (dBm) signal magnitude at the input of an amplifier, the gain of the amplifier drops by 1 dB from its linear (small-signal) gain value.

1.3.2 Intermodulation Distortion

Intermodulation Distortion (IMD) is an important consideration for transceiver linearity and Spurious Free Dynamic Range (SFDR). It is characterized by a two-tone test, where two closely-spaced in-band frequencies of equal intensity (say, P_{in} dBm) are applied at the input of the nonlinear block. These two frequencies mix within the block to generate not only the amplified fundamental frequencies at the output (say, P_{out_1st} dBm), but also two closely space spurious tones (third-Order products) that are impossible to filter out, as shown in Figure 7. IMD is quantified by the metric Third-Order Intercept Point (IP3). If the power of the output spurious tones is assumed to be P_{out_3rd} dBm, the input-referred IP3 (IIP3, in dBm) is given by:

$$IIP3 = P_{in} + \frac{P_{out\_1st} - P_{out\_3rd}}{2} \tag{4}$$

To mathematically understand the two-tone test, let us assume two closely spaced frequencies ω_1 and ω_2 of similar amplitude are incident at the input of an amplifier. The input sinusoid can be defined $x(t) = A\cos(\omega_1 t) + A\cos(\omega_2 t)$. Using the input-output relation described in equation 2, the output partially is

$$y(t) = \left(k_1 A + \frac{3k_3A^3}{4} + \frac{3k_3A^3}{2}\right)\cos\omega_{1,2}t + \cdots \quad (Fundamental\ Term)$$

$$+\frac{3k_3A^3}{4}\cos\left(2\omega_{1,2} - \omega_{2,1}\right)t + \cdots \quad (3^{rd} order\ Intermod)$$

$+ \ldots .$ (5)

From the above output expression 5, *dc* offsets and harmonics have been neglected to maintain compactness. The intent is to show the reader the appearance of $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ frequencies at the output. These are called the third-order intermodulation terms. The problem with these two spurious signals is that they are close to the frequencies of interest ω_1 & ω_2, and cannot be filtered out. These tones have the potential to fall in pass-bands of other circuits in the vicinity and cause interference. A pictorial description of the concept discussed above is shown in Figure 8 below.

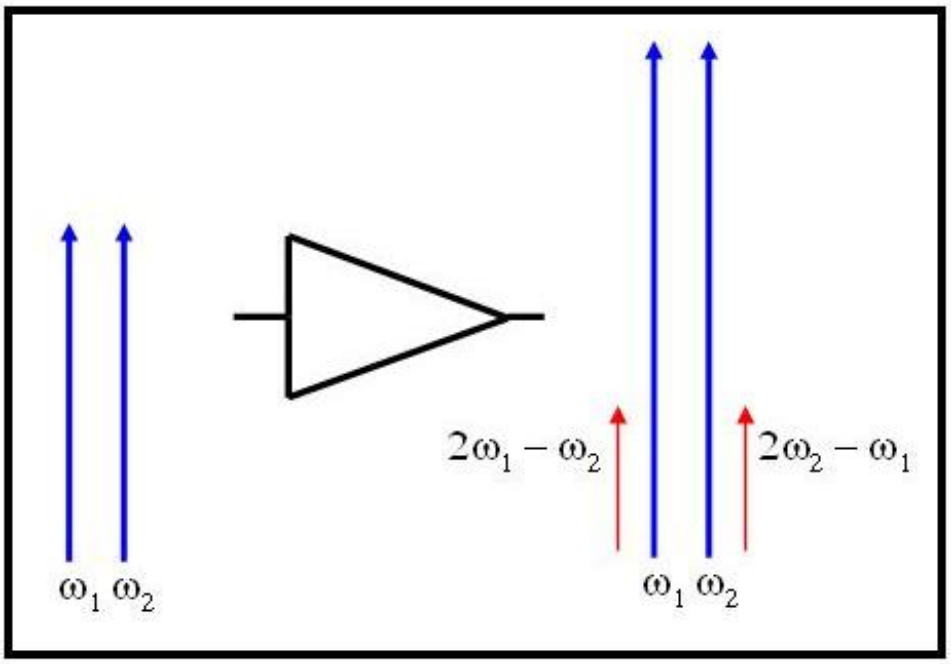

Figure 8: Amplifier outputs for 2 closely spaced input frequencies.

A simpler version of Figure 7, this time showing P1dB too, is shown in Figure 9. For small but increasing input signal with amplitude A, the fundamental output grows linearly (as also derived in expression 5, neglecting higher order terms for small inputs). The 3rd order intermodulation term, however, increases cubically. Plotted on a decibel power scale, the fundamental tone grows with a 1:1 slope with input signal power, and

the 3rd order intermodulation grows with a 3:1 slope (due to its cubic dependency on input signal).

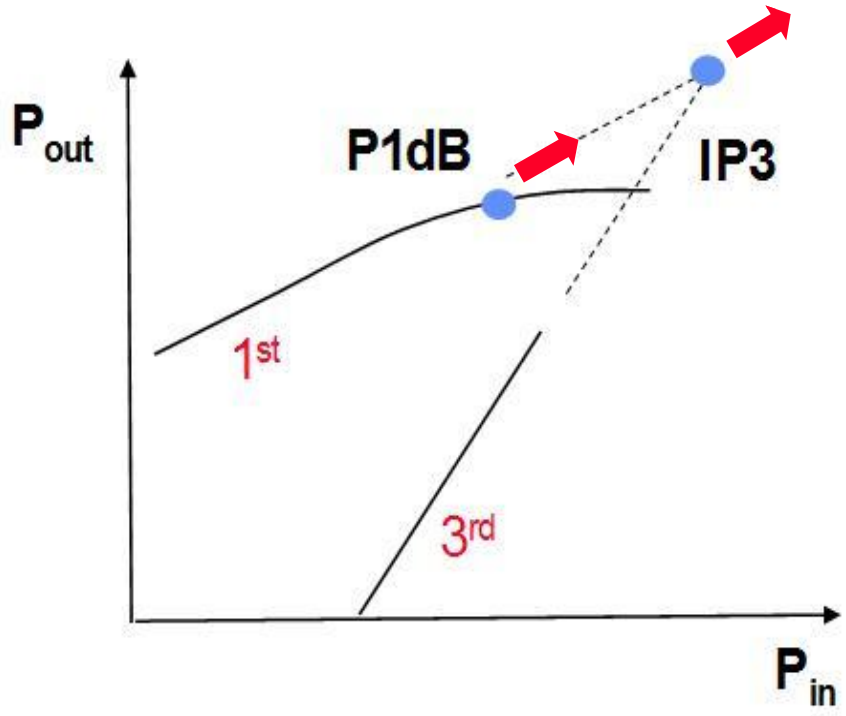

Figure 9: Fundamental (1st) and 3rd order intermodulation (3rd) outputs as a function of increasing input signal power P_{IN}.

To enable clarity of display, only 2 output frequencies are shown in Figure 9 instead of the 4 output frequencies of an amplifier as shown in Figure 4. This is because the signal amplitudes for the two fundamental are similar, as is the case for the 3rd order intermodulation terms (as seen from equation 5). P1dB is the point where the fundamental output stops growing linearly with the input signal and gain compression sets in (described in section 1.2.1). The hypothetical extensions and intersection of the fundamental output curve and the 3rd order intermodulation output curve gives us what is called the 3rd order Intercept Point (IP3), and is the benchmark by which amplifier linearity is quantified. The x-coordinate of IP3 is known as the Input Third-Order Intercept Point (IIP3), and the y-coordinate of IP3 is known as the Output Third-Order

Intercept Point (OIP3). IIP3 and OIP3 are very key figures of merit, and will be used extensively in this work to quantify linearity.

1.8 Organization and Contributions of the Dissertation

This dissertation investigates the possibility of using complementary SiGe HBTs for designing high-performance RF front-ends, with a specific focus on the dynamic range of SiGe-based front-ends. The dissertation also explores novel methods such as biasing SiGe HBTs in weak-saturation to obtain aggressive circuit performance metrics under constraints of *dc* power consumption.

Chapter II sheds light on the linearity and reliability aspects of complementary SiGe HBTs. The performance of electrically-matched (similar f_T and breakdown-voltage) *npn* and *pnp* SiGe HBTs is compared after extensive measurements and analyzed using device physics. It was found that the *pnp* SiGe HBTs not only have a better linearity performance than *npn* HBTs under similar *dc* power consumption, they also operate more reliably under very-large-signal RF conditions. This result was totally unanticipated, and was published for the very first time, cementing the supremacy of *pnp* SiGe HBTs as engines driving high-performance RF circuit design. The work presented in this chapter has been published in [1] and [2], and a journal extension is being prepared for submission to Transactions of Electron Devices.

Chapter III discusses the dynamic range considerations that circuit designers have to address when designing high-performance RF front-ends. Special attention has been given to the enhancement of dynamic range. A novel method to enhance the large-signal linearity of RF switches and circuits, using SiGe HBTs in inverse mode of operation, is discussed [6]. Methods to lower the noise-floor, hence enhancing the signal dynamic range, are investigated in the context of cryogenic mixed-signal circuits [7]. Lastly, compact modeling considerations for predictive RF circuit, with a focus on dynamic range, are also addressed in this chapter [3].

Chapter IV intends to bridge the gap from device physics to circuit design in the context of high-performance RF circuit design. A novel method to use a SiGe HBT in power-constrained RF circuits, known as weak-saturation, is described. This study is published in [4]. Thereafter, the same principle of weak-saturation is used to fabricate a high-performance X-Band Low Noise Amplifier. This amplifier has the highest gain per *dc* power consumed amongst all other published X-Band LNAs. The LNA is published in [5].

Chapter V describes the design of a high-performance SiGe cellular band quadrature modulator for use in base-station applications. The modulator has the highest linearity compared to other existing upconverting modulators in the market or in the literature. A Gilbert cell to realize the frequency mixing, followed by a variable gain amplifier to boost the gain, was used to obtain a simulated OIP3 of 30 dBm and a conversion gain of 17.7 dB for a 3 GHz LO tone. The chip is currently under fabrication.

Lastly, chapter VI concludes the dissertation with a summary of the contributions, and a discussion on possible future work that might result as an offshoot of this work.

CHAPTER II

COMPLEMENTARY SIGE HBTS: LINEARITY AND RELIABILITY

2.1 Introduction

Complementary SiGe HBT (*npn* + *pnp*) IC platforms represent the leading edge in high-performance analog/mixed-signal IC design platforms. They enable very high speed and low power bias references, and efficient push-pull driver stages. Therefore, electrically-matched (similar f_T and breakdown voltages) *npn* and *pnp* SiGe HBTs should, in principle, enable RF and microwave circuits with similar performance as III-V HBT circuits, but at the fraction of their cost.

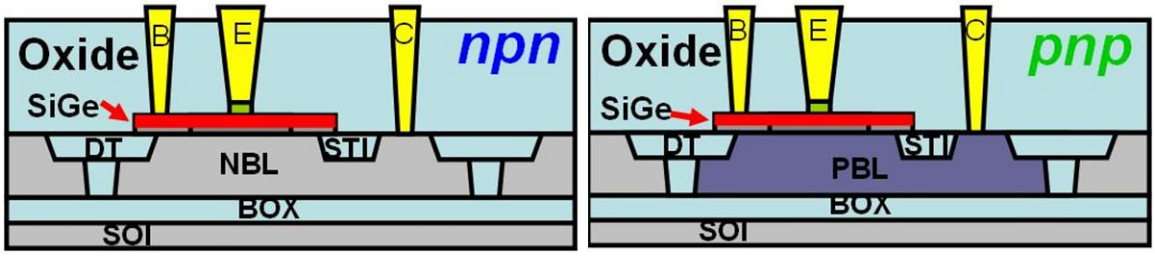

Figure 10: A block-diagram of complementary SiGe HBTs on thick-film SOI.

It is a challenge to fabricate structurally similar, electrically matched *npn* and *pnp* SiGe HBTs. In part, the challenge stems from the fact that holes, as a majority carrier, are about two orders of magnitudes slower than electrons acting as majority carriers [22]. This happens because of the higher effective mass of holes, as compared to electrons. In terms of saturation velocity, which is the maximum velocity a charged carrier can attain in presence of an electric field, the holes are about 25% slower than electrons. This poses a problem for the fabrication engineers trying to build a *pnp* HBT similar in speed to an *npn* HBT. The best way to circumvent this issue is to intentionally make the *npn* HBTs slower (which, with proper lateral [23] and vertical [24] scaling, currently attain near-terahertz speeds at room temperature), so they can operate at the same speed as *pnp* SiGe HBTs.

There have been some attempts at engineering a complementary SiGe BiCMOS process with a fast *pnp* SiGe HBT. A good example [25] incorporates a fast *pnp* SiGe HBT, which, however, is not electrically matched to the *npn* HBT in the same process. This issue has now been resolved [16] by the CBC-8 process, which is truly a matched complementary SiGe process. A block-diagram of the complementary SiGe HBTs used in this work is shown in Figure 10. Both devices incorporate shallow- and deep-trench isolation, and are fabricated on top of a high-resistivity silicon substrate with a buried oxide (BOX). As a rough estimate, the cost of including extra lithography masks for manufacturing the *pnp* SiGe HBTs is approximately 15% greater than the costs involved in making an *npn*-only BiCMOS process. In return, the added expenditure in creating a C-SiGe process can enable a whole host of new applications such as faster active loads, faster pull-up devices, high efficiency low dropout regulators, full rail-to-rail amplifiers, and balun-less transceivers. All of these circuits that can be enabled by C-SiGe technologies are significantly reduced in their occupied die areas.

The objective of this work is to comprehensively evaluate both linearity and reliability of *npn* and *pnp* SiGe HBTs. The motivation is to investigate the underlying physical mechanisms which produce differences in distortion and reliability performances between *npn* and *pnp* SiGe HBTs over varying stimulus conditions (e.g. geometry, *dc*-bias, etc). The aim of this work is to aid understanding of how C-SiGe platforms can be leveraged to design high-performance RF front-ends and improved mixed-signal circuits.

2.2 Linearity of Complementary SiGe HBTs

2.2.1 Motivation

Conventionally, *npn* SiGe HBTs have been the transistor of choice for high-performance RF front-end design. In this work, the intermodulation performance

(discussed in Section 1.3.2) of complementary SiGe HBTs in [16] is evaluated. The normalized *ac* response of these standard sized SiGe HBTs is shown in Figure 11. For their high gain and pervasiveness in amplifier circuits, we chose to examine SiGe HBTs operated in a common-emitter (CE) topology.

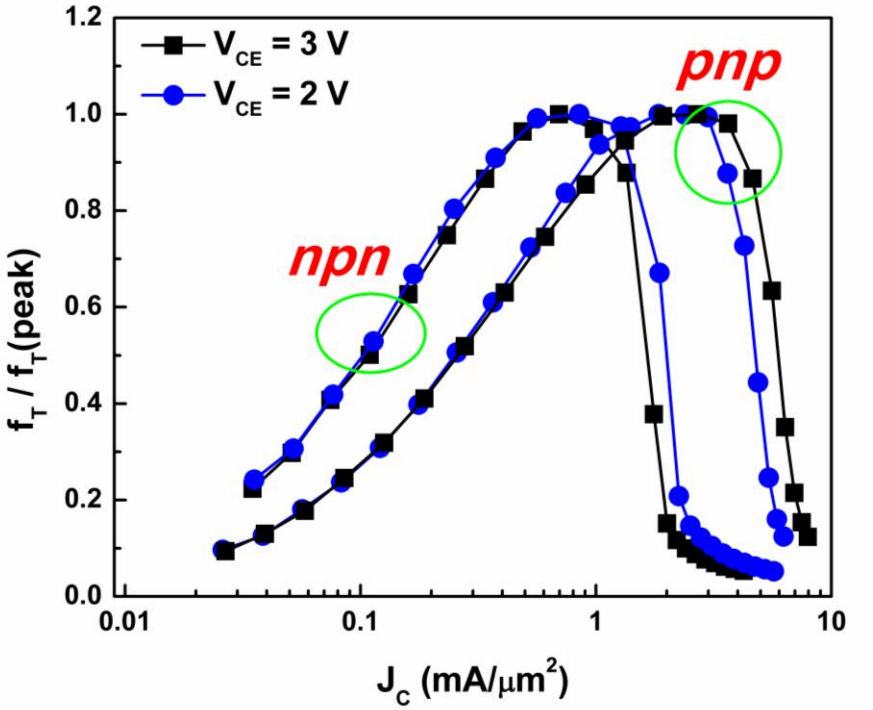

Figure 11: Cut-off frequencies (f_T) normalized to peak f_T of the npn and pnp SiGe HBTs vs. current density (J_C).

2.2.2 Experimental Details and Measured Results

Two-tone measurements, as described in Section 1.3.2, were performed using a Maury load-pull system at room temperature. The two RF tones were summed in a power combiner and were applied to the standard sized DUT, with *dc* bias being controlled by bias-tees at both the input and output terminals. A spectrum analyzer was used to measure P_{FUND} and P_{3rd} to obtain IIP3 and gain. The test set-up is described in detail in [26]. Measurements were performed over bias and geometry at 2.8 GHz, 5.0 GHz and 9.5 GHz, with 10 MHz tone spacing.

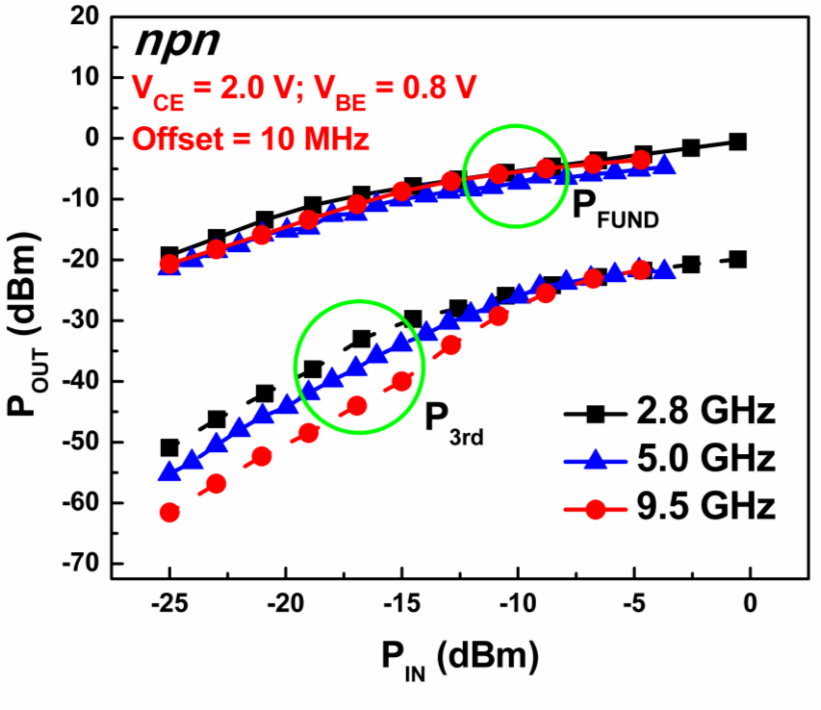

Figure 12: Fundamental power (P_{FUND}) and 3rd order intermodulation (P_{3rd}) as a function of input power for a standard sized npn SiGe HBT.

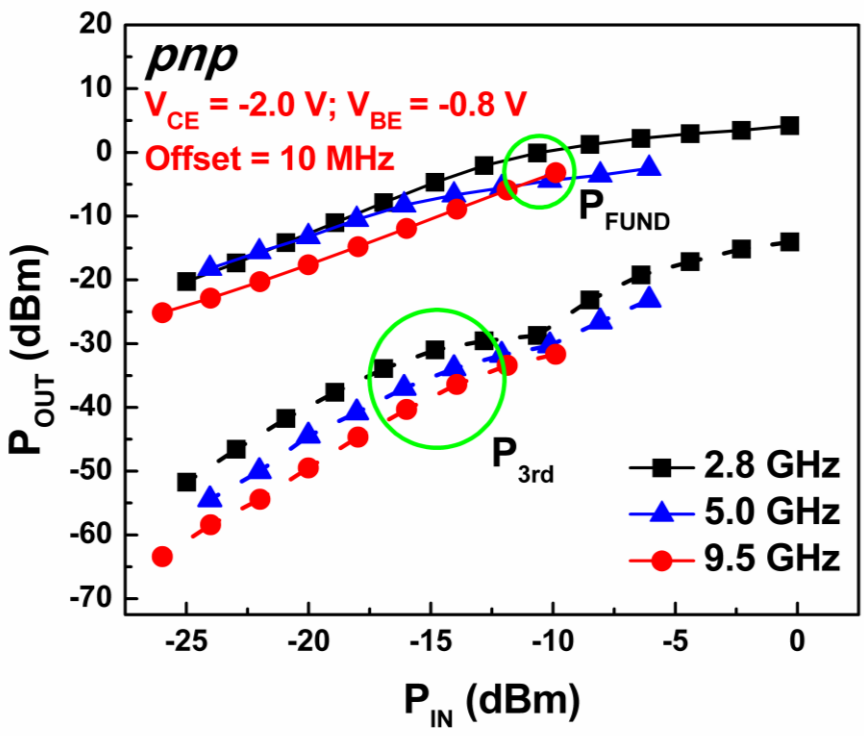

Figure 13: Fundamental power (P_{FUND}) and 3rd order intermodulation (P_{3rd}) as a function of input power for a standard-sized pnp SiGe HBT.

To gain a better understanding of the underlying distortion mechanisms of these complementary SiGe HBTs, and to maintain consistency in comparison over different device geometries, biases (V_{CE} = 0.5 – 3V with varying I_C), and device topologies (*npn* vs. *pnp*), 50 Ω terminations were used as starting points for the source and load impedances. After understanding the linearity response of the DUT with 50 Ω terminations, the effects of conjugate load matching on the linearity of the *npn* and *pnp* SiGe HBTs were investigated. Two-tone measurements were performed on complementary SiGe HBTs with the load impedance matched for highest gain at 5 GHz, at a source impedance of 50 Ω.

Figures 12 and 13 illustrate results of the two-tone analysis (f_1 and f_2) of sweeping input power (P_{IN}) for fixed bias on the standard sized *npn* and *pnp* SiGe HBTs, respectively. For small input signal V_{IN}, the amplitude of fundamental output (f_1) is proportional to V_{IN}, and the amplitude of third-order intermodulation term ($2f_2 - f_1$) is proportional to V_{IN}^3 [12], and their corresponding power levels show a 1:3 slope (P_{FUND} : P_{3rd}), as expected. All load-pulls and bias sweeps were performed at input power levels where this 1:3 slope was observed.

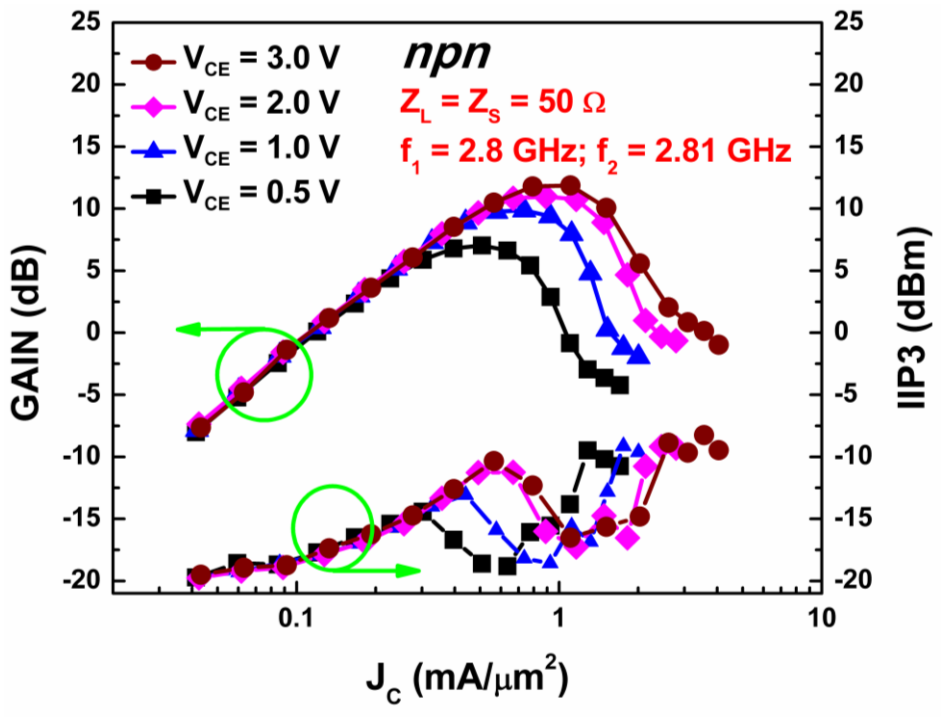

Figure 14: IIP3 and gain vs. current density (J_C) with increasing V_{CE} for a standard-sized npn SiGe HBT.

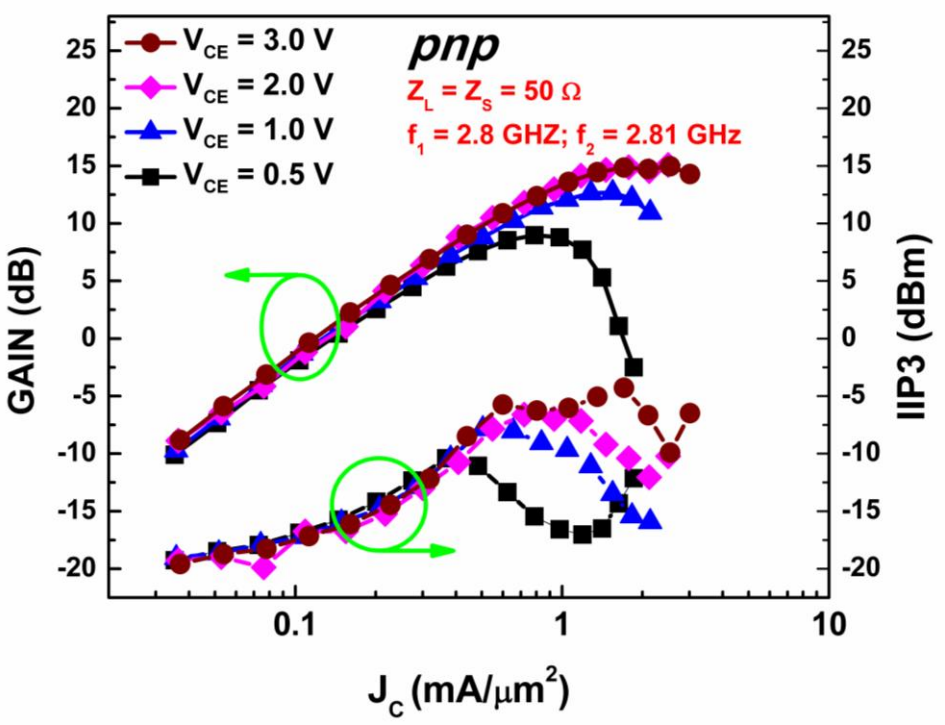

Figure 15: IIP3 and gain vs. current density (J_C) with increasing V_{CE} for a standard-sized pnp SiGe HBT.

Figures 14 and 15 show the results of two-tone measurements on standard-sized *npn* and *pnp* SiGe HBTs with increasing I_C and V_{CE}. For low V_{CE}, a very low reverse bias is being applied across the collector-base (CB) junction, and hence the Kirk Effect onset can degrade the gain, according to following equation in [27]:

$$J_K = q v_{sat} N_C \left[1 + \frac{2\varepsilon(V_{CB} + \varphi_{BI})}{q N_C {W_{epi}}^2}\right], \tag{6}$$

where v_{sat} is the carrier saturation velocity, N_C is the collector doping density, V_{CB} is the reverse bias across the CB junction, φ_{BI} is the built-in junction potential, and W_{epi} is the width of collector epi-layer. With increasing V_{CE} (and hence V_{CB}), the onset current density for Kirk Effect (J_K) is delayed, and thus we observe higher gains at higher current densities. This trend is consistent across both *npn* and *pnp* SiGe HBTs.

In terms of IIP3 performance, a large reverse bias (high V_{CE}) yields improved linearity performance, since the collector is more fully depleted [28-30]. For a fully-depleted epi-layer, the width of the depletion region becomes a constant equaling W_{epi} (distance from CB junction to the sub-collector), and hence the capacitance of the reverse-biased CB junction (C_{CB}) becomes independent of any increase in voltage applied across its terminals. Since the rate of change of C_{CB} with respect to changing V_{CB} is the dominant source of nonlinearity in the high current region [12], this effect loses its dominance for increasingly depleted collector epi-layers. Hence, the peak IIP3 values improve with increasing V_{CE}.

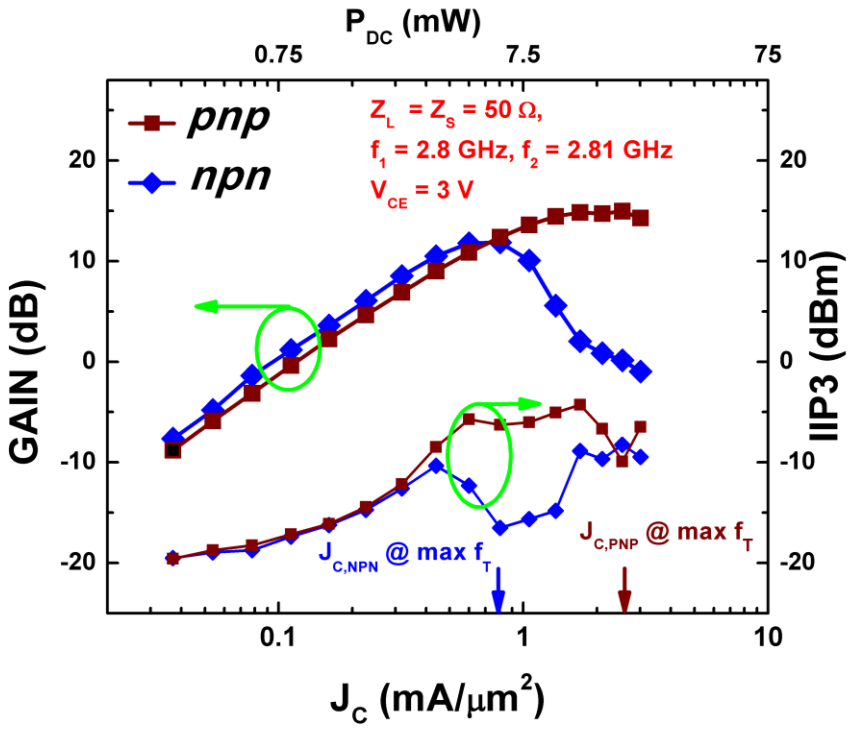

Figure 16: IIP3 and gain vs. current density (J_C) with fixed bias for a standard sized npn and pnp SiGe HBT.

Figure 16 shows the results of two-tone measurements for standard-sized *npn* and *pnp* SiGe HBTs at similar bias. To highlight the role of Kirk effect onset in the gain roll-off, current density values for maximum f_T at the same bias are marked for both *npn* and *pnp* SiGe HBTs.

The basic physical mechanisms surrounding the optimal design of complementary SiGe HBTs with similar performance can explain the observed differences in linearity performance between the *npn* and *pnp* SiGe HBTs. For identical doping profiles and lateral geometry, *npn* SiGe HBTs will outperform *pnp* SiGe HBTs, since electrons have a higher mobility due to their reduced effective mass. To compensate for this, one needs to dope the collector of the *pnp* SiGe HBT more heavily than for the *npn*. From a breakdown voltage (BV) perspective, one can do this without BV loss, given that the hole impact ionization rates are lower than for electrons, and the current gain of the *pnp* will be smaller than for the *npn*. Doping the collector more heavily has direct impact on the

linearity performance of *pnp* SiGe HBTs, since higher N_C makes the C_{CB} more resistant to changes in V_{CB}, improving linearity for similar applied bias, consistent with data shown in Figure 16.

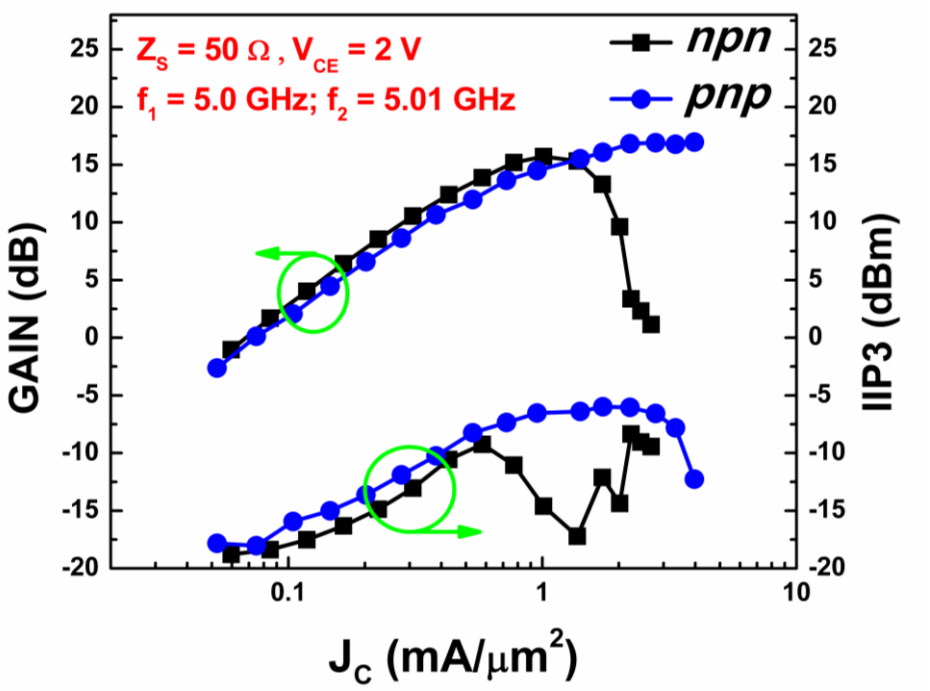

Figure 17: IIP3 and gain vs. current density (J_C) with fixed bias for a standard sized npn and pnp SiGe HBT under conjugate load matching.

The devices were also measured under the case of conjugate load matching for standard-sized *npn* and *pnp* SiGe HBTs, at 5 GHz, since that is usually the load at which transistors will be terminated in an RF circuit. The results of this measurement are shown in Figure 17. It was observed that the matching point for both *npn* and *pnp* SiGe HBTs was in the high impedance region ($Z_{L,pnp}$ = 144 + j*137, $Z_{L,npn}$ = 187 + j*166). Even though improved gains were observed for both devices, the general trends remained as shown in Figure 16. The linearity performance under matched impedance remained similar to the 50 Ω termination case.

2.2.3 Analysis

In the previous section, a qualitative method of nonlinearity estimation and comparison was discussed. The goal of this section is to analyze the differences in linearity of *pnp* and *npn* SiGe HBTs using the Volterra Series method of mathematical calculations. The Volterra Series (VS) analysis is a mathematical tool that can be used to model weak nonlinearities in a distortive system [31-33]. Conceptually very similar to the power series expansion, Volterra series is used in cases where predicting memory-effects (where inductive, capacitive elements interact with the signal) is crucial, e.g. power amplifiers [34]. The author has already developed a framework for distortion analysis using Volterra Series [35], so only key points of the algorithm will be repeated.

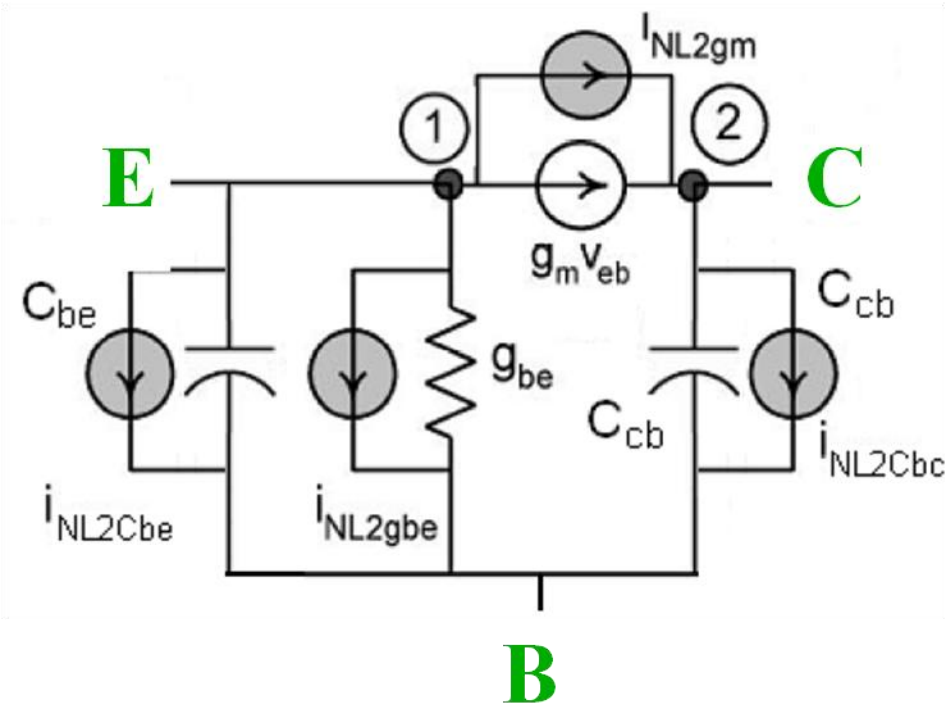

Figure 18: Simplified equivalent π-circuit of npn SiGe HBT, with the four major sources of nonlinearities, as well as their associated 2nd–order nonlinearity contributing current sources.

The four major sources of nonlinearity in a SiGe HBT (g_m, g_{be}, C_{CB}, and C_{BE}) are shown in Figure 18. Also shown are the nonlinearity causing current sources (i_{NL2X})

associated with each of the four sources of nonlinearity. A very simplified method of calculating the nonlinearities using Compact Modified Nodal Analysis [36] (CMNA) generated by this circuit are discussed in [12], with greater levels of complexities addressed in [35].

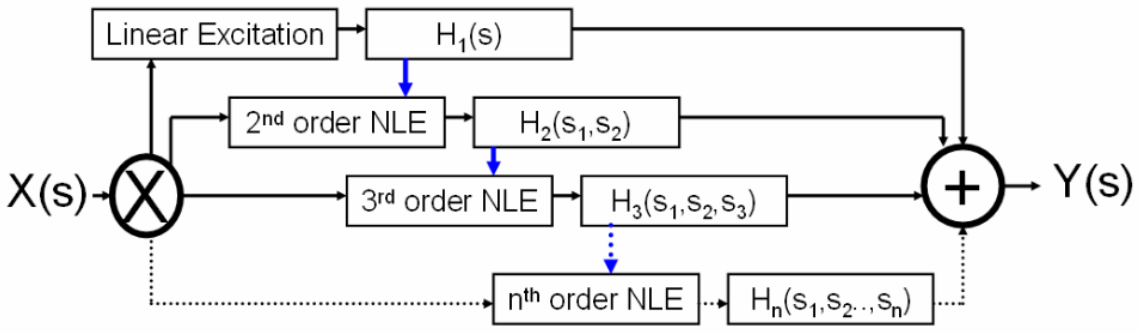

Figure 19: A pictorial representation of the algorithmic flow of Volterra Series.

The flow of the Volterra Series algorithm is shown in Figure 19. *X(s)* is the input to the circuit, and $H_1(s)$ is the basic transfer function of the linearized circuit. *X(s)* multiplied with $H_1(s)$ forms the linearized part of the output *Y(s)*. However, the output of the linearly excited stage also forms the input for the 2nd order nonlinear excitation (NLE), which interacts with the 2nd-order transfer function $H_2(s_1,s_2)$ to create the 2nd-order part of the output *Y(s)*. This output term, in turn, forms the input for the 3rd order nonlinear excitation, and so on. For an input fundamental signal of amplitude *A*, the linear fundamental output can be denoted by

$$V_{fundamental} = A * H_1(j\omega_1), \tag{7}$$

and the third-order intermodulation term can be denoted by

$$V_{IM3} = \frac{3}{4}A^3 * H_3(j\omega_1, j\omega_1, -j\omega_1). \tag{8}$$

From Figure 7, IIP3 can be defined as the extrapolated point where the magnitudes of the fundamental and the third-order intermodulation terms become equal. This would imply that the intercept point can be determined by equating equation 7 to

equation 8. Doing so, the voltage of the input signal at which the third-order intercept point (IP3) can be determined is

$$A_{IP3} = \sqrt{\frac{4}{3}\frac{|H_1(j\omega_1)|}{|H_3(j\omega_1, j\omega_1, -j\omega_2)|}}. \quad (9)$$

The algorithm in Figure 19, as well as the equations emanating from it, was implemented using MATLAB (the script is attached in the appendix). Very close agreement was found between the IIP3 values predicted by the Volterra Series calculator and the Harmonic Balance simulation engine that is found in commercial circuit simulators such as Spectre.

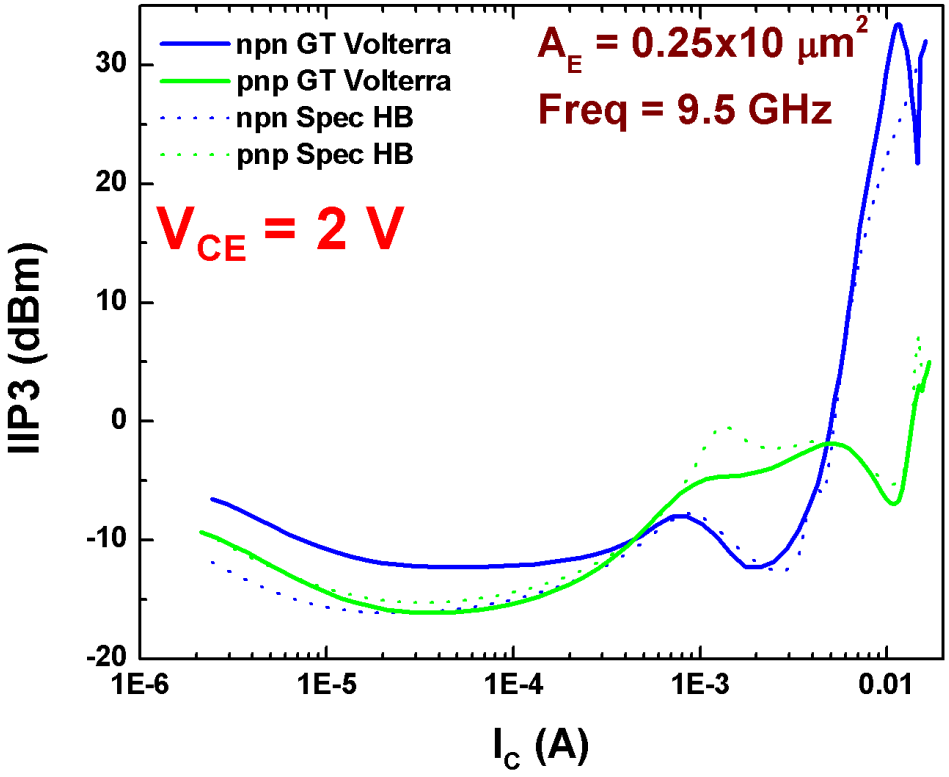

Figure 20: A comparison of the IIP3 values predicted by both a commercial simulator (Spectre), as well as the Volterra Series calculator implemented at GT using MATLAB.

Figure 20 shows the comparison of the IIP3 values that were predicted by two sources – the Harmonic Balance (HB) simulator in Spectre, and the Volterra Series

calculator implemented using MATLAB, for both *npn* and *pnp* SiGe HBTs. For the comparison, the Spectre HB simulations were considered as the gold standard, and agreement with HB simulations was considered a good test of Volterra Series algorithm fidelity. The inputs to the Volterra MATLAB program were *dc* currents, as well as depletion and diffusion capacitances C_{BC} and C_{BE}. The *dc* current inputs were taken from the HBT compact model, and the capacitances were extracted from simulated S-parameters using the framework developed in [37]. It can be seen that within the range of usable collector-current values, the HB and Volterra simulations agree to a very large extent. This is a good sign, as it allows us to delve inside the device to study the individual internal nonlinearity causing source.

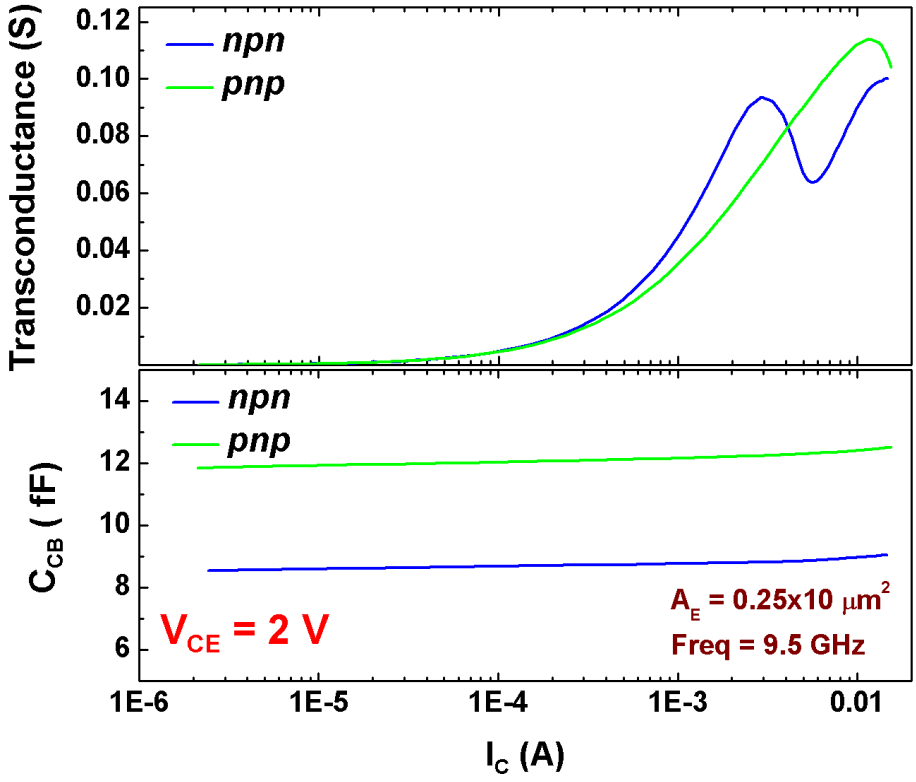

Figure 21: Extracted transconductance, as well as depletion capacitance C_{CB} for both the npn and pnp SiGe HBTs.

Figure 21 shows the extracted transconductance, as well as the depletion capacitance C_{CB} for both *pnp* and *npn* SiGe HBTs using the Volterra series calculator. Since g_m and C_{CB} are the two dominant sources of nonlinearity in SiGe HBTs [12], they

were made the focus of this analysis. It was mentioned earlier that to fabricate electrically matched complementary SiGe HBTs, the *npn* HBT is intentionally slowed down. This is achieved by doping the collector with a lower dopant density (N_C). Said in other words, the collector doping density in the *pnp* SiGe HBTs is higher than that in the *npn* SiGe HBT to compensate for the slower majority holes. Correlating this with equation 6 of the dissertation, it becomes immediately apparent why the onset of Kirk effect is delayed in the *pnp* SiGe HBT, where the transconductance starts to roll off at a much higher I_C compared to the *npn* SiGe HBT. Higher collector doping (N_C) also translates into a higher C_{CB} depletion capacitance, which is also observed in Figure 21.

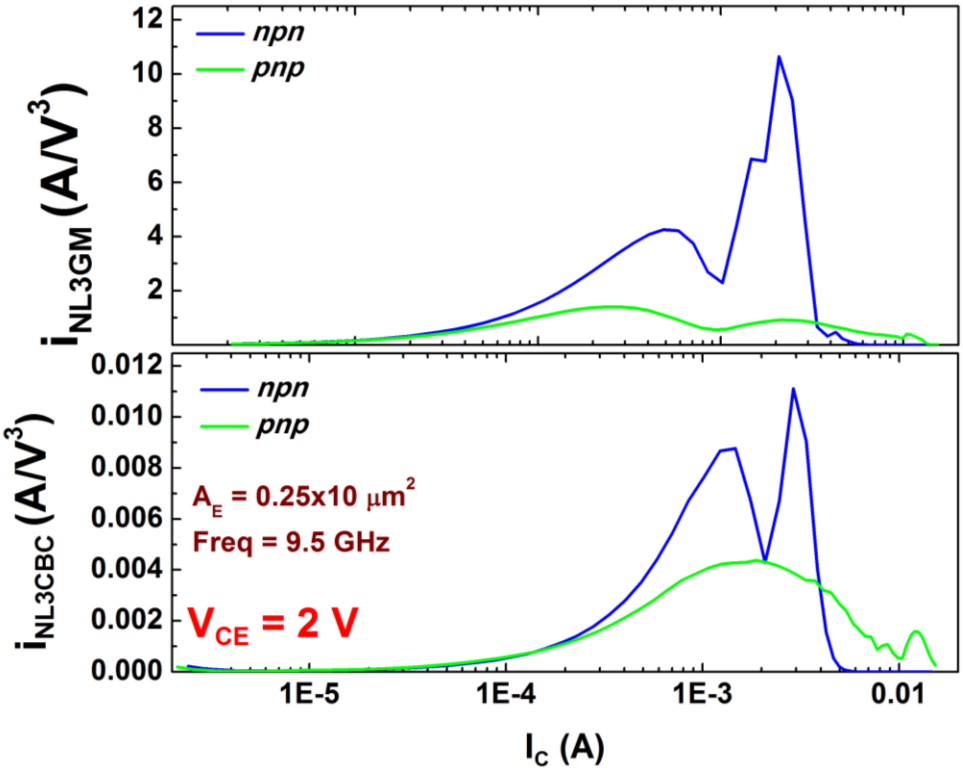

Figure 22: A comparison of the 3rd order nonlinearity current sources for two major sources of nonlinearity in SiGe HBTs – g_m and C_{CB}.

Figure 22 compares the 3rd order nonlinearity current sources i_{NL3CBC} and i_{NL3GM}, which are the nonlinearity current sources for two major sources of distortion in SiGe HBTs – g_m and C_{CB}. The smaller the value of i_{NLX} current source, the lesser its

contribution will be to overall linearity (IIP3) of SiGe HBT. Because of a very linear g_m vs. I_C trend in the case of *pnp* SiGe HBT (as seen in Figure 21 too), its 3rd order nonlinearity source i_{NL3GM} is much smaller in value compared to the *npn* SiGe HBT [32]. Since g_m nonlinearity is the main source of distortion in SiGe HBTs, and Figure 22 establishes that g_m nonlinearity is much smaller in *pnp* SiGe HBTs compared to *npn* SiGe HBTs, it follows automatically that the *pnp* SiGe HBT will have a higher IIP3 than a similarly sized *npn*. All this can be related back to the fact that the collector is doped much higher in *pnp* SiGe HBTs. It is also seen that the capacitive nonlinearities due to C_{CB} depletion capacitance are much smaller in *pnp* SiGe HBT, although the overall i_{NL3CBC} values are much smaller than the values generated by g_m nonlinearity source i_{NL3GM}.

2.2.4 Summary and Implications

An analysis of RF linearity in complementary SiGe HBTs was presented in this section. It was observed that in the low current region, both *pnp* and *npn* devices exhibit similar linearity performance. In high current region, however, the onset of Kirk effect is delayed in the *pnp* devices due to a higher collector doping density, due to which the *pnp* SiGe HBTs are able to achieve greater linearity and gain. This has direct implications for mixed-signal circuit design, since it enables the design of highly linear circuits using complementary (or even *pnp* only) circuit topologies.

2.3 Reliability of Complementary SiGe HBTs

2.3.1 Motivation

The reduced cost and compact size of SiGe technologies enable their use in highly-integrated transmit-receive (T/R) modules needed in radar and communication systems, which have historically been the bastion of III-V solutions. SiGe-based power

amplifiers (PA), providing nearly one-watt output power at X-Band, have already been demonstrated for use in such T/R modules [38]. The question to ask ourselves is: what is the impact of the interactions of such high-power circuits squeezed into a highly integrated T/R module? While a lot of research on reverse emitter-base [39, 40] and mixed-mode *dc* stresses [41] exists in literature, no literature exists on the impact of near-damaging RF power stress on SiGe HBTs. This becomes especially interesting in the context of complementary SiGe HBTs on SOI. This is the first work to investigate the robustness of complementary SiGe HBTs under very large-signal conditions.

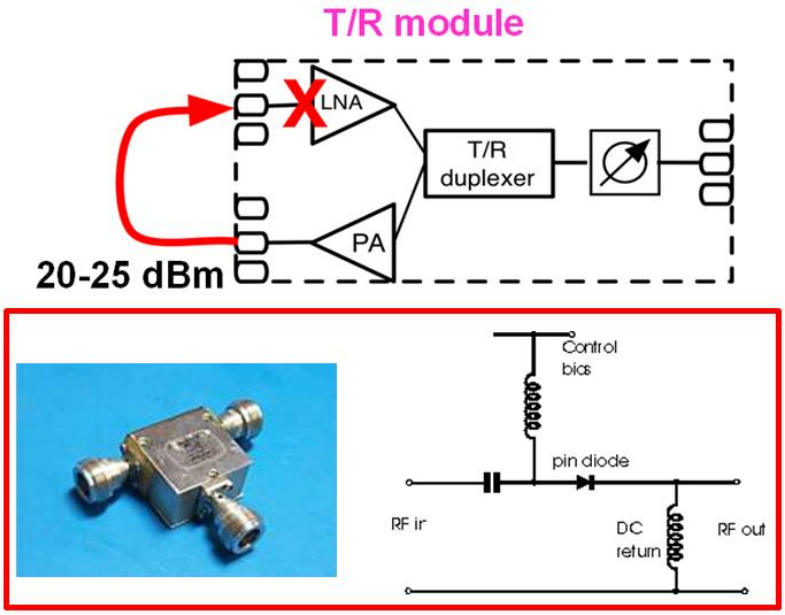

Figure 23: (Top) A possible damage mechanism in a T/R module, with high power levels from LNA leaking into other circuits. (Bottom) Existing methods of limiting power levels in RF systems.

Figure 23 shows a plausible scenario where very high power levels from the PA can leak into other sensitive parts of the highly-integrated MMICs. Although RF switches ideally prevent leakage of such high RF power from the transmit path into the receive paths, their failure under continuous RF stress would expose the receiver front-end (specifically the LNA) to very large RF powers [42]. There exist other solutions such as a power limiter, or a high-breakdown diode, also shown in Figure 23. These solutions are

not perfect since the limiter cannot be integrated on a chip and a diode based solution is very lossy. It thus becomes imperative for the system designer to understand the levels and duration of RF stress a front-end can survive before damage and catastrophic failure occurs.

The motivation behind this work is to compare the intrinsic reliability of *npn* and *pnp* SiGe HBTs under high RF stress, for potential usage in RF front-ends, shedding light on the underlying failure mechanisms such as electromigration and "non-classical punchthrough." Several conclusions can be drawn from this study that can enable the system designer to design more robust front-ends. The *pnp* SiGe HBTs are shown, for instance, to better withstand aggressive RF stress, buying us larger Time-to-Failure (TTF) for the T/R modules. In light of these advantages that *pnp* SiGe HBTs can offer designers, a case is made for the potentially improved RF system performance by utilizing *pnp* SiGe HBTs in RF front-end design.

2.3.2 Experimental Details

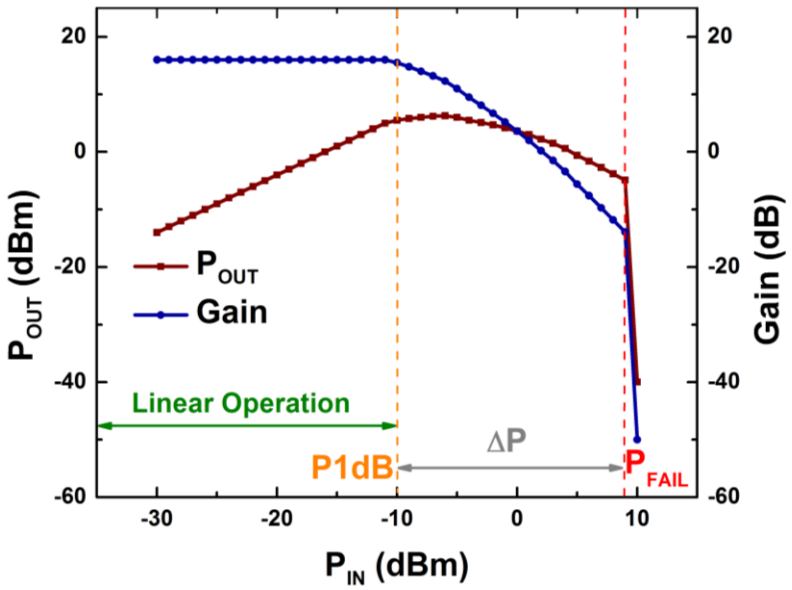

Figure 24: A representative reliability measurement, where an increasing input power was applied to the SiGe HBT to a point where RF gain values saw a very sharp and sudden decline.

The transistors investigated are *npn* and *pnp* SiGe HBTs on thick-film SOI, with matched electrical performance [16]. Two variants of *npn* SiGe HBTs – a low breakdown (LVNPN) and a high breakdown (HVNPN) version – and a high breakdown *pnp* SiGe HBT (HVPNP) are investigated. HVNPN and HVPNP devices have similar f_T and BV_{CEO}. All devices–under-test (DUT) were similarly sized (A_E = 0.25 x 20 μm^2) and had similar metallization schemes to facilitate comparisons. All the transistors examined were operating in Common-Emitter (CE) mode, due to its high gain and ubiquity in amplifier circuits. The measurement setup used in this experiment is described in detail in [43]. In Figure 24 a representative reliability measurement on the SiGe HBTs is shown. The input power was increased much beyond the P1dB to a point where the RF gain values saw a sharp and sudden decline. At that point (P_{FAIL}), the device was considered dead, and unusable.

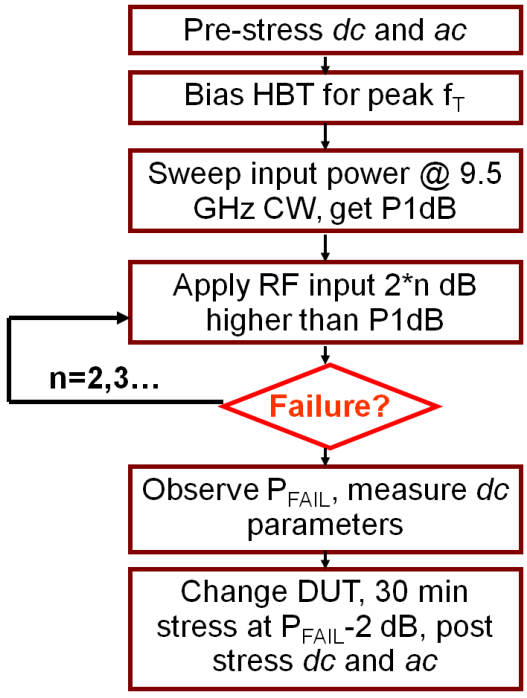

Figure 25: A flowchart of the reliability measurement algorithm.

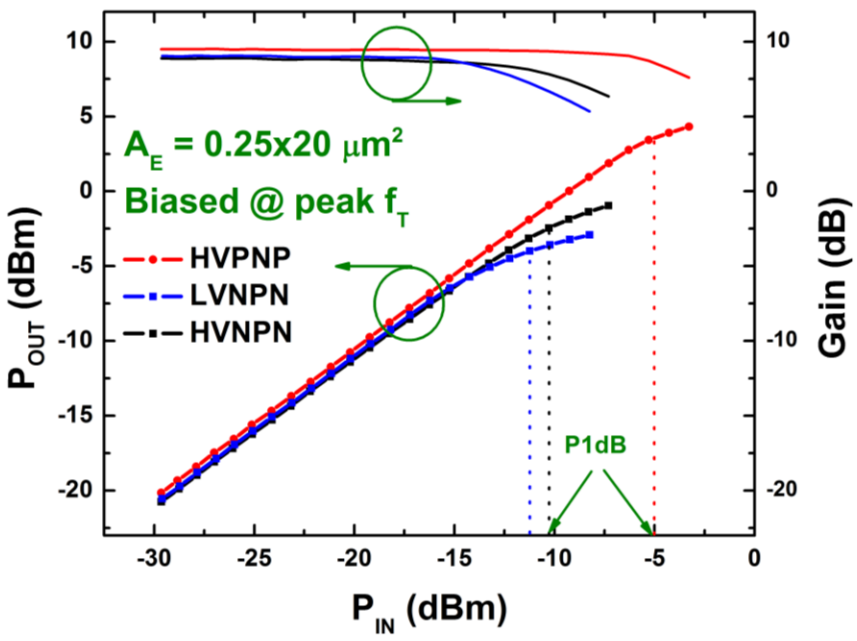

Figure 26: P_{OUT} and Gain for 3 different DUTs all biased at peak f_T for a 9.5 GHz CW input tone under 50 Ω terminations.

Figure 25 shows the flowchart of the reliability measurement algorithm. The general measurement methodology was to determine and bias the SiGe HBT close to peak f_T (V_{CE} = 3.0 V for HVNPN and HVPNP, V_{CE} = 1.5 V for LVNPN), and measure the P1dB of the HBT for a 9.5 GHz CW input tone under 50 Ω source and load terminations, as shown in Figure 26. Pre-stress *dc*, *ac*, and RF parameters (at a steady state input power of -30 dBm) were determined. Next, RF power was applied using a 9.5 GHz CW tone, which was then stepped upward by 2 dBm starting from the P1dB point. The DUT was then stressed for 60 sec at each input power level. Post-stress *dc*, *ac*, and RF parameters were measured. The RF power at which the DUT instantly failed (P_{FAIL}) was determined, and device was stressed at a power level 2 dBm backed off from P_{FAIL} for 30 minutes. After this 30 minute stress, the full suite of DUT parameters was then re-measured. Multiple devices were measured to ensure repeatability of the results (typical results are shown).

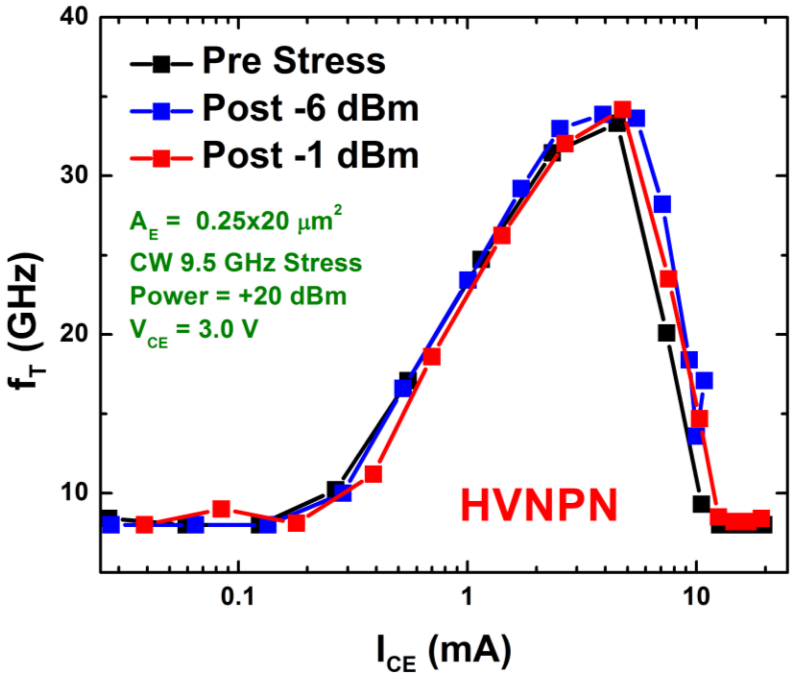

Figure 27: Pre- and post 60 sec stress f_T for small increments in input RF power.

2.3.3 High Power Stress Results

A. HVNPN

The P1dB for HVNPN (V_{CE} = 3.0 V) was found to be -11 dBm. Increasing the RF input power incrementally and stressing for 60 sec yielded no significant change in the device characteristics. This is also shown in Figure 27, where the f_T characteristics remain unchanged after stresses of -6 dBm and -1 dBm. Continuing this process, the P_{FAIL} of the HVNPN was found to be +22 dBm (158 mW, 7.9 V pk-pk at 50 Ω). As soon as P_{FAIL} is applied to the DUT, the Collector-Base (CB) junction appears to be irreversibly shorted due to avalanching carriers. We can dub damage process 'non-classic punchthrough failure' since this effect is irreversible unlike for the reversible 'classic punchthrough'.

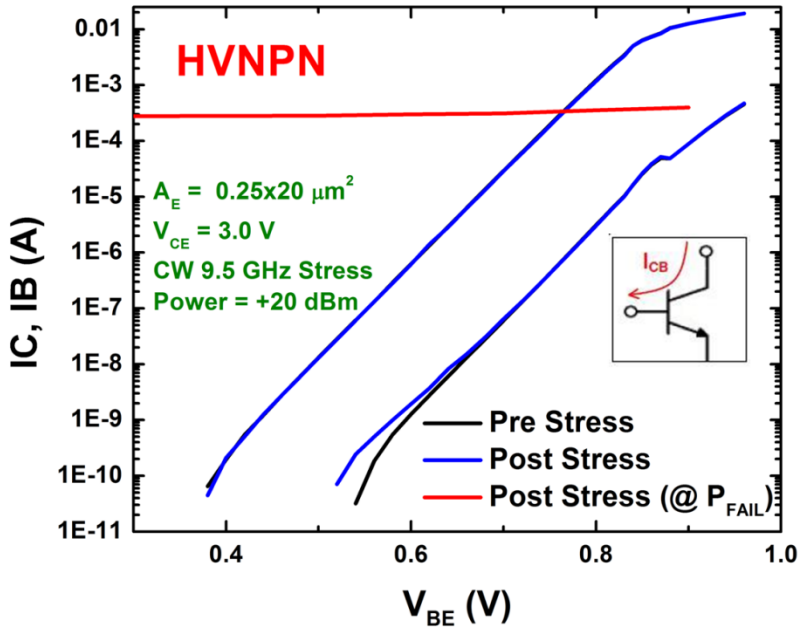

Figure 28: Comparison of the Gummel characteristics of HVNPN pre and post +20 dBm stress after 60 sec, and after applying P_{FAIL} (where IC and IB become coincident).

As with classical punchthrough, voltage control over the collector current is lost, rendering the transistor useless. This is shown by the red curve as well as the inset in Figure 28, which shows the measured post-stress Gummel characteristics of the HBT. Some post-stress leakage in the base-current (I_B) was observed. This behavior appears to be consistent with the mixed-mode damage mechanism, where hot carriers in the C-B space charge region create interface traps in the E-B spacer, which are responsible for higher non-ideal I_B due to increased recombination [44]. No observable change in the collector current (I_C) is seen, indicating no change in series resistance at the collector and emitter. The post 60 sec stress f_T characteristics remain unchanged, indicating no post-stress change in internal capacitances. This was also observed in [45]. Overall, the device is able to withstand 60 sec of +20 dBm RF stress without showing catastrophic failure.

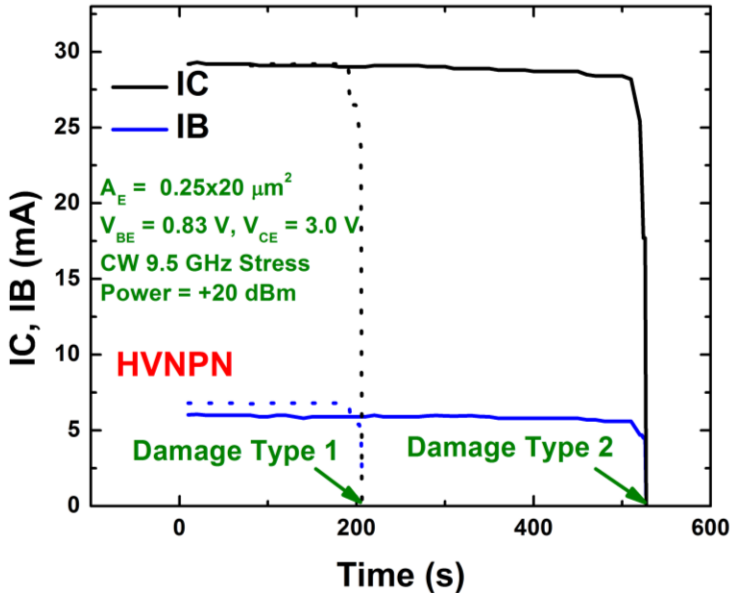

Figure 29: Time-to-Failure highlighting two different damage mechanisms in the HVNPN.

Next, the DUT was stressed for duration of 30 minutes. Two kinds of damages were observed, each being onset at a different time after input RF power was applied to the device. This time to failure and the associated mechanisms are shown in Figures 29 and 30. Definite trends were seen in both modes of failure. First, no HVNPN device ever survived the 30 minute stress it was subjected to. Second, as seen clearly in Figure 29, the DUT currents remain nearly constant until only a few seconds before failure. In all cases the failure was not gradual with time; rather, it was sudden and catastrophic.

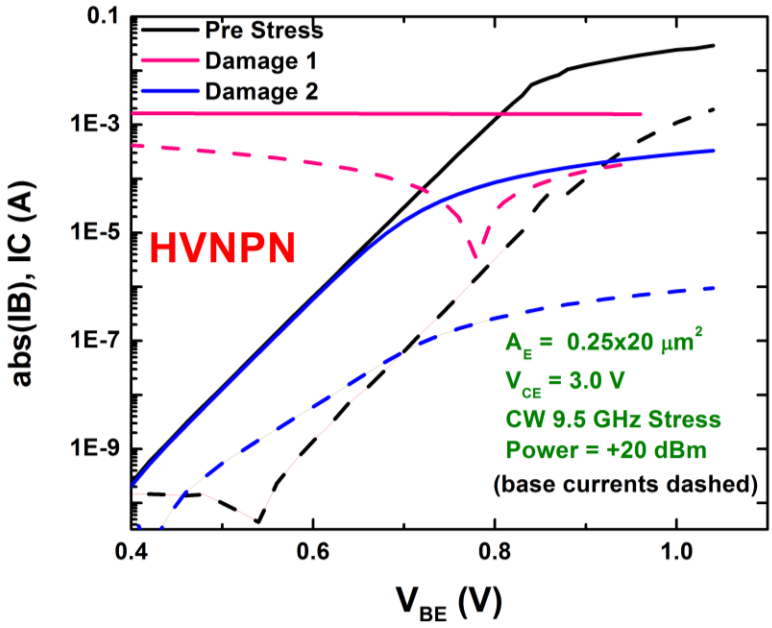

Figure 30: Gummel characteristics showing different failure mechanisms in the HVNPN after 30 min RF stress.

Figure 30 shows the post-damage Gummel characteristics, and it is apparent that differing damage mechanisms are at play in the DUT. 'Damage Type 1' usually set in within 2-3 minutes of applying RF stress. Its electrical signature is very similar to the 'non-classical punchthrough' seen also in Figure 16 when P_{FAIL} was applied. 'Damage Type 1' is clearly correlated with process parameter variations, as some HBTs may be catastrophically damaged at input powers slightly lesser than P_{FAIL}. The E-B junction appears to be intact post death, although there is significant leakage at low V_{BE} due to G/R traps introduced by stress.

'Damage Type 2', on the other hand, onset usually after 9-10 minutes of applied RF stress. Here, the electrical signature points towards an increase in collector or emitter series resistance (the Gummel characteristics flatten at higher V_{BE}), which is likely due to the metal to semiconductor contact failure due to the large currents flowing through the

DUT under stress. In addition, enhanced I_B leakage is also observed. Both damage mechanisms are permanent, and the device is rendered unusable.

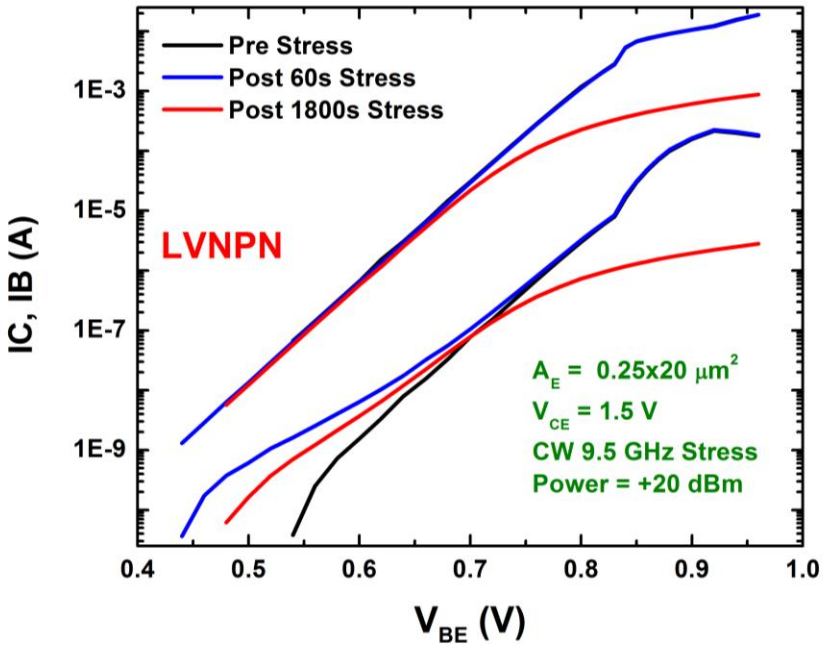

Figure 31: LVNPN Gummel characteristics pre- and post- 20 dBm stress.

B. LVNPN

The high-performance, low-breakdown version of the *npn* SiGe HBT (LVNPN) in this process was subjected to RF stress in a similar manner to that described above. The P_{FAIL} of the LVNPN was experimentally determined to be +22 dBm. From the pre- and post-stress Gummel characteristics (Figure 31), it can be seen that there is only excess I_B leakage observed post 60 sec stress. When subjected to a 30 min stress, the DUT fails around 25-28 minutes of stress. The DUT always turns very resistive, in a similar manner to the 'Damage Type 2' for the HVNPN case, suggesting a metallization failure (Figure 30). Post 60 sec stress, f_T remained unchanged, since capacitances did not change with stress, as was also confirmed in [45].

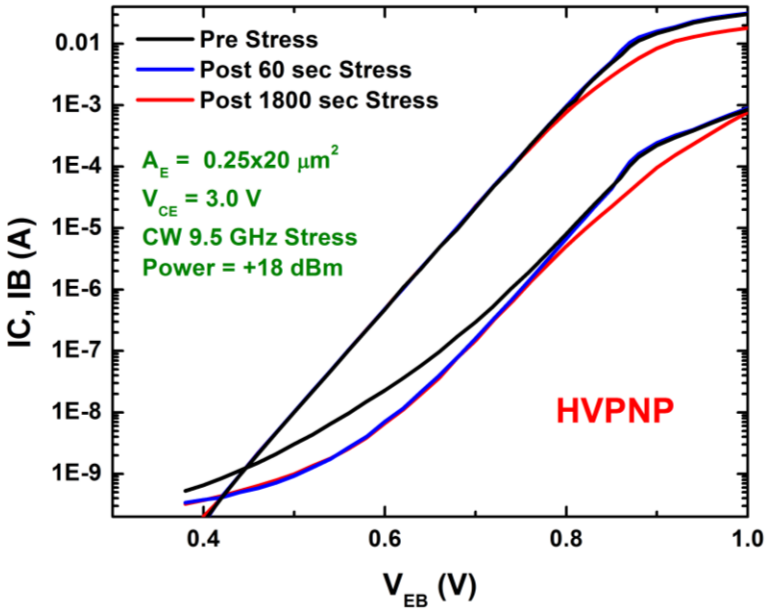

Figure 32: HVPNP Gummel characteristics before and after 18 dBm stress.

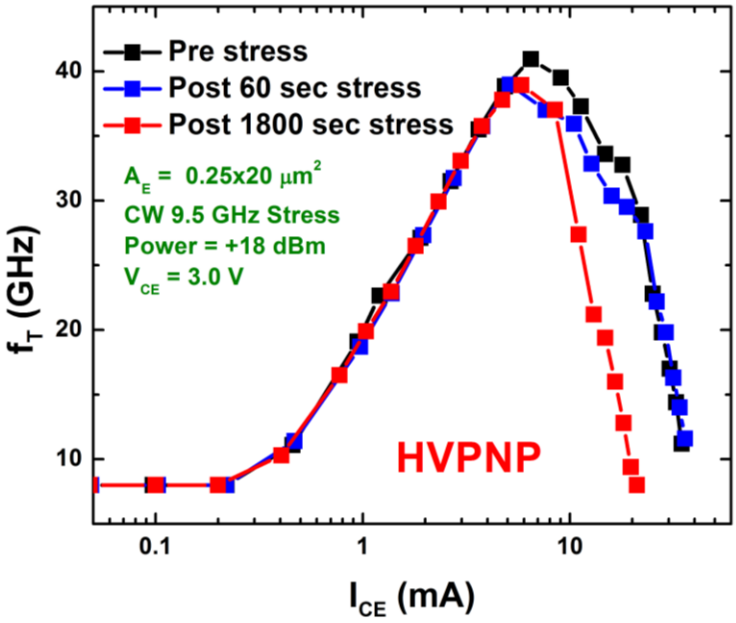

Figure 33: HVPNP f_T characteristics before and after 18 dBm stress.

C. HVPNP

The P_{FAIL} of the HVPNP was determined to be +20 dBm after testing multiple

devices. Figure 32 shows the Gummel characteristics before and after 60 sec and 30 min RF stress of the DUT. It is clear that the device does not undergo failure in a manner seen in previous two *npn* SiGe HBTs. Some resistive increases are seen post 30 min stress, but they remain minor compared to the *npn* SiGe HBT. The electrical signature of increased series resistance post-stress is seen in the f_T curves as well, (Figure 33). In summary, the *pnp* SiGe HBTs repeatedly survived a stress of 30 minutes without losing functionality substantially better than for the aggressively stressed *npn* SiGe HBTs, making them potentially attractive for use in RF front-ends that might be exposed to large RF input signals.

It is interesting to note that the base currents in the *pnp* SiGe HBTs (Figure 32) consistently decrease (improve) with applied RF stress. This phenomenon is unique to the stressed *pnp* transistors, where electrons are the minority carriers, and was also observed in [46]. The speculation is that hot electrons jump over the barrier at the Si-SiO_2 interface around the emitter-extrinsic base region and are trapped within SiO_2. In *npn* devices, however, minority holes are attracted to the surface, which recombine with electrons via interface traps, hence the increased current following stress. In the *pnp* devices, however, the trapped electrons repel the minority electrons, thus reducing this recombination mechanism, and hence leading to decreased base currents with stress

2.3.4 Analysis

Table 1: A summary of DUT average currents and gain, before, during, and after 60 sec stress.

HVNPN	Pre-Stress	Under-Stress	Post-Stress
I_C (mA)	3.4	**29.2**	3.4
I_B (mA)	0.01	**5.9**	0.01
Gain (dB)	8.9	**-17.3**	8.9
LVNPN			
I_C (mA)	3.1	**30.3**	3.1
I_B (mA)	0.08	**8.5**	0.08
Gain (dB)	9.3	**-15.4**	9.3
HVPNP			
I_C (mA)	6.9	**35.9**	6.9
I_B (mA)	0.06	**4.16**	0.06
Gain (dB)	9.64	**-6.00**	9.66

Table 1 summarizes the average currents of all the DUTs before, during, and after stress. High RF power self-biases the DUT during stress, producing very large terminal currents. These large currents are likely to cause metallization fatigue and ultimately failure. The fact that the DUTs are fabricated on SOI substrates enhances the effects of self-heating, yielding degraded thermal response compared to bulk substrates.

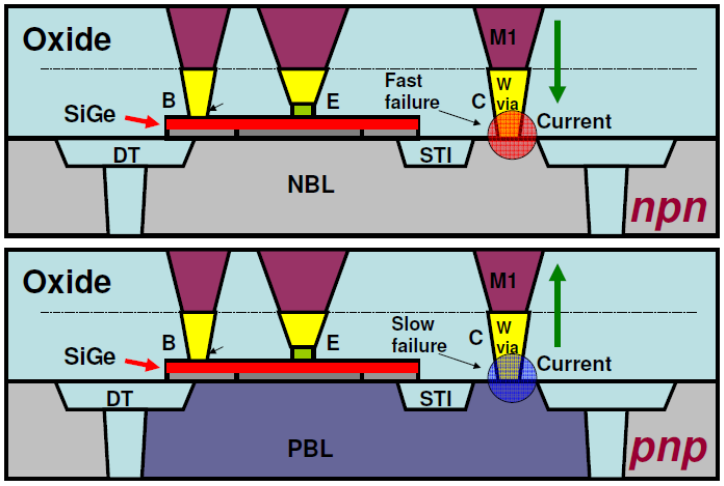

Figure 34: Pictorial representation of the failure mechanisms. Top and bottom devices are npn and pnp SiGe HBTs, respectively.

An interesting question to consider is: why is the *pnp* SiGe HBT more resilient to metallization failure under RF stress compared to the *npn* SiGe HBT? A study performed in [47] sheds light on this observed phenomenon. As stated above, the series resistance of the devices is increased due to applied RF stress. Since all devices (*npn* and *pnp*) share the same metallization scheme and contacts to the collector (i.e., tungsten plugs), this suggests that the origin of the differences lies in the nature of the current flow through the device. As shown in Figure 34, in a *pnp* HBT, the current flows OUT of the collector, and in an *npn* HBT, it flows INTO the collector. It was shown in [47] that the mean time-to-failure of a tungsten-filled via is almost an order of magnitude larger when electrons flows from Metal-2 to Metal-1 (the case of the *pnp* SiGe HBT) than when it is the other way around (the case of the *npn* SiGe HBT). These results are consistent with our observations. In addition, a logical explanation for why the metal lines are able to carry current exceeding their limits (in this case, roughly 2 mA/μm width) is as follows: since the current flowing through the structures is an *ac* current, the damage from one cycle of the current is rapidly reversed (undone) by the next (opposite) cycle (assuming a classical electromigration process). Thus, the electron "wind" is not unidirectional under *ac* stress, but is instead a cyclical bi-directional wind. Hence, the metal lines are able to withstand

far larger current density than is specified in the process manuals, which are determined/defined by *dc* measurements

2.3.5 Summary and Implications

This work presents, for the first time, results of applying aggressive levels of RF stress on complementary SiGe HBTs on thick-film SOI. It was seen that the *pnp* SiGe HBTs are able to withstand substantially larger stress than the *npn* SiGe HBTs. Analysis based on differences in metallization failure is furnished to augment the measured results. This investigation suggests that in certain mixed-signal circuit applications (e.g., RF front-ends), complementary (or *pnp* only) circuit topologies may well prove advantageous in terms of not only linearity, as described in the previous section, but also in terms of robustness and reliability.

CHAPTER III

HIGH DYNAMIC RANGE CONSIDERATIONS

3.1 Introduction

Dynamic Range (DR) is a key consideration for receiver-side circuits. Usually expressed in dB, DR is the ratio of the largest and the smallest values of a signal that a receiver-side circuit, such as LNA, can detect and amplify. For RF circuits, dynamic range is often described as the ratio of the largest possible undistorted sine wave to the root-mean-square noise-floor amplitude level. Since expanding the dynamic range usually comes at the expenditure of increased *dc* power consumption, a few novel techniques are discussed in this chapter that aim to enhance DR without increasing the overall power budget of the receiver.

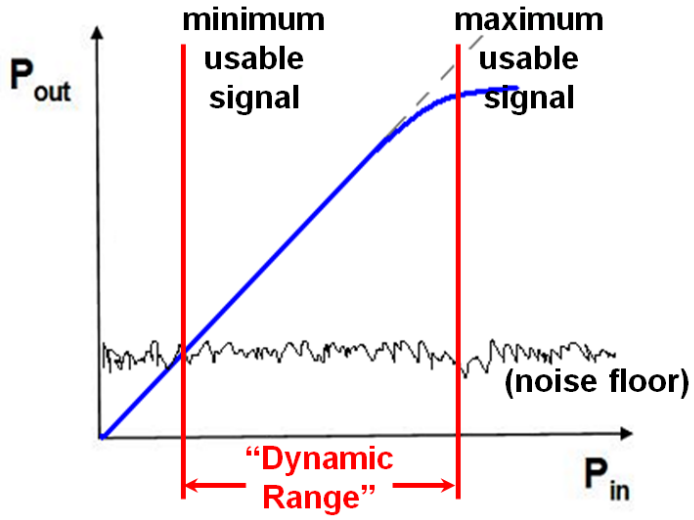

Figure 35: Receiver Dynamic Range is the ratio between maximum usable signal (compression) and minimum usable signal (Noise floor) in dB.

Figure 35 shows a pictorial representation of the DR of a receiver. The lower end of the receiver dynamic range is the noise floor, which also happens to be the minimum usable signal by the receiver. The noise floor for RF circuits can either be modulated thermally, or by crosstalk interference from other circuit blocks that share the same

silicon substrate. The upper end of the DR is limited by the onset of signal compression, which is the maximum "usable" signal of the receiver. The metric to quantify DR is known as "Spurious Free Dynamic Range" (SFDR), which is the ratio of the fundamental signal power to the power of the strongest undesirable frequency spurs in the output. An expression to calculate SFDR (in dB) is given as:

$$SFDR = \frac{2(IIP3 - F)}{3} - SNR_{min}\,, \tag{10}$$

where Signal-to-Noise ratio (SNR) SNR_{min} corresponds to minimum SNR requirements for the system [48]. "IIP3" corresponds to the Input-referred Third-order Intercept Point, and "F" denotes the noise floor level of the receiver in dBm.

This chapter will focus on three main dynamic range considerations: enhancing the upper end of the dynamic range spectrum (compression limited), reducing the lower end of the dynamic range spectrum (noise limited), and investigating the correct compact-model to use for predictive high dynamic-range RF front-end design. In Section 3.2, an RF switch is used as a test circuit to demonstrate a novel method to mitigate signal compression. This work is under review in IEEE Transactions on Electron Devices [6]. In Section 3.3, techniques are identified to limit crosstalk noise in cryogenic mixed-signal ICs. The work in this section is under review in IEEE Transactions on Electron Devices [7]. In Section 3.4, two major next-generation compact models for SiGe HBTs, VBIC [49] and HICUM [50], are compared against measured linearity data to identify the compact model of choice for predictive RF circuit design. This work was published in [3].

3.2 Addressing Large-Signal Linearity Concerns

3.2.1 Case Study: Enhanced Linearity RF Switch

RF switches, while conceptually very simple, play a very crucial role in the overall front-end performance. Often times, the performance of the front-end system can

be limited by the performance of the RF switches used in it. In reconfigurable systems, RF switches are used to dynamically turn-on and turn-off transistor cores that increase/reduce the overall linearity of the system. In the case of an integrated on-chip transceiver, RF switches connect the antenna to either the transmit or the receive path. For such systems, RF switches need to be robust and show a much delayed onset of signal-compression. If the RF switch connecting the power amplifier to the antenna starts to compress before the PA does, it clearly limits and hinders the performance of the whole system. Recent work demonstrating watt-level PAs using SiGe has established SiGe [38] as a key commercial platform for use in robust, large-signal transmitters. Since the high output power of the PA has to be handled by on-chip RF switches, there has recently been a slew of publications focusing on the topic of on-chip high-power RF switches using III-V [51], commercially available CMOS [52],and SiGe technologies [53]. In [53], it was shown that a SiGe HBT operated in inverse mode (i.e., electrical emitter and collector flipped) may offer higher linearity than traditionally used forward-active mode, but that work did not present a framework for understanding the results. This section significantly advances those initial data by developing an analytical framework to understand the differences in performance of SiGe HBT RF switches operating in forward and inverse modes, and by suggesting that the power handling capability of such SiGe RF switches can be further optimized by suitably modifying the Ge and doping profiles.

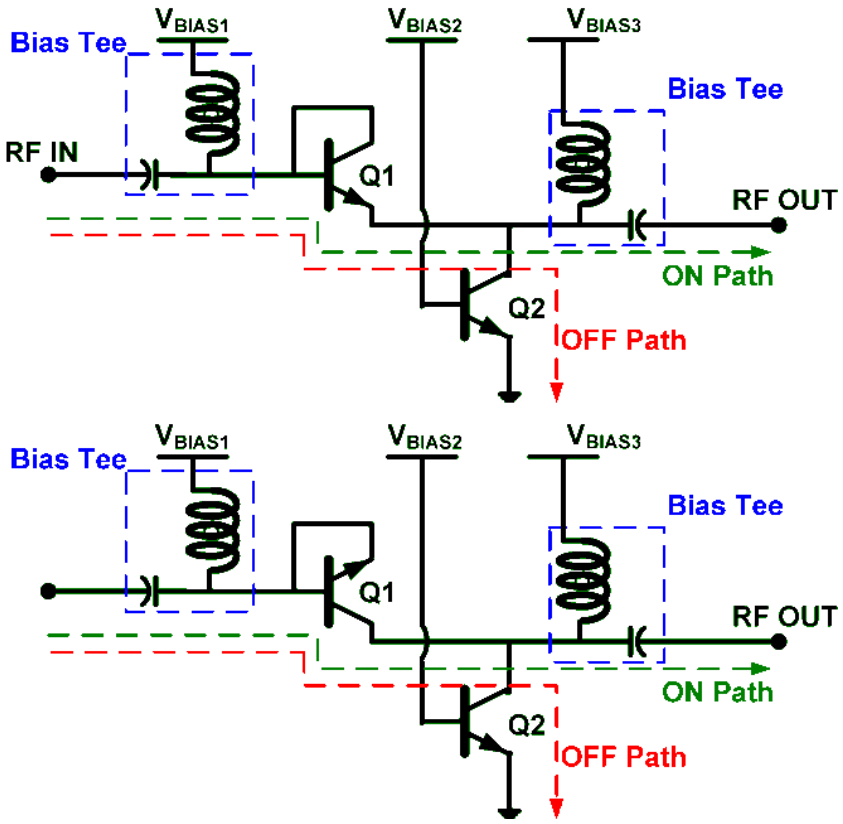

Figure 36: A schematic of the forward- and inverse-mode SiGe HBT RF switches. The OFF state SiGe HBT Q2 is identical for the two topologies.

3.2.2 Switch Design and Measured Results

A. Switch Design

Four separate Single-Pole-Single-Throw (SPST) switches were designed with the goal of comparing their power handling capabilities in the ON state. As shown in Figure 36, the series ON path consisted of only a single SiGe HBT (Q1), and was actuated by tuning voltages V_{BIAS1} and V_{BIAS3}. Two different types of SiGe HBTs, the high-voltage (HV) and low-voltage (LV) *npn* [16], were used as Q1 in both forward and inverse [54] modes of operation. To enable an apples-to-apples comparison, both HV and LV *npn* devices were sized to 0.25x10 μm^2. Thus, a conscious choice was made to not minimize the small-signal insertion loss of the SPST switch in the ON state. Both SiGe HBTs have

identical base-emitter junctions; however, the LV *npn* leverages an additional selectively implanted collector (SIC) to achieve f_T values greater than 50 GHz. The SIC also reduces the extrinsic collector resistance of the LV *npn* compared to the HV *npn*. The OFF state shunt HBT (Q2) in each switch was a LV *npn* sized to be 0.25x10 μm^2, and was actuated by V_{BIAS2} and V_{BIAS3}. The measurement configuration included high power bias-tees (Auriga AU0699-0004) on the input and output ports for decoupling the *dc* bias and *ac* inputs.

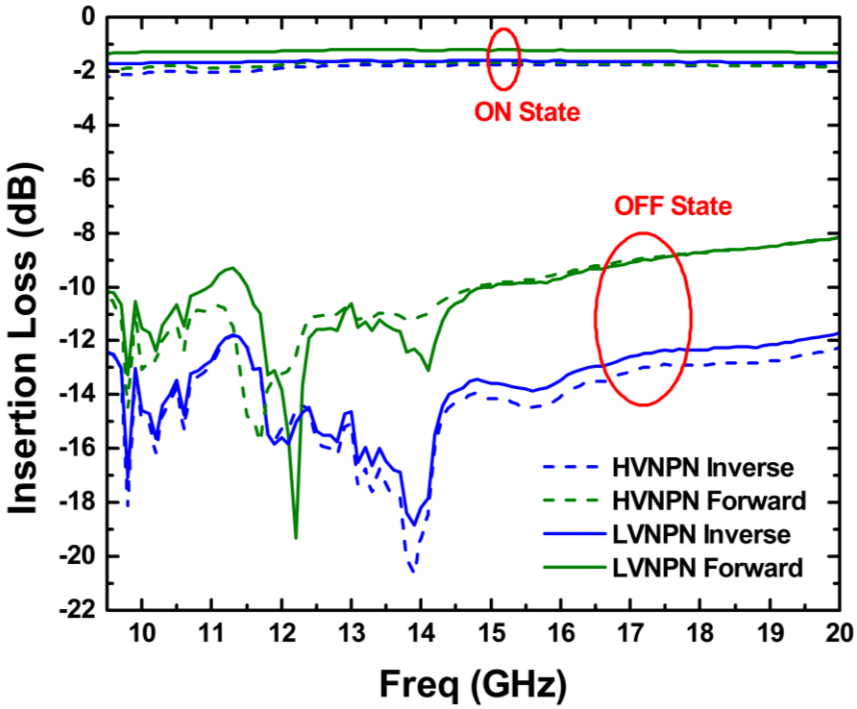

Figure 37: Measured small-signal insertion loss of the forward and inverse-mode npn SiGe HBT RF switches.

B. Measured Results

Figure 37 shows the measured small-signal insertion loss (IL) of the switches in the ON and OFF state, with 50 Ω input and output impedances. For all four SPST switches, the ON state IL lies in the sub-3 dB range (again, this was unoptimized for the present study, and the IL loss for each switch can be minimized by optimizing the

geometry of HBT Q1). In the OFF state, however, stark differences in IL are observed over frequency. For forward-switches (with Q1 in forward mode), the IL was 3-4 dB higher than the inverse-switches, thus making the inverse-switches attractive for use as high-isolation switches in OFF state.

The difference in OFF state IL for the inverse-switches stems from the doping in the physical collector-base junction of the SiGe HBT. The capacitance in a p-n diode junction under zero *dc* reverse-bias can be approximated by the standard expression [22]:

$$\boldsymbol{C_{jo} \propto \sqrt{\left(\frac{N_a * N_d}{N_a + N_d}\right)}}, \tag{11}$$

where N_a and N_d are the acceptor and donor doping densities, respectively. Since $N_{d\_collector} << N_{d\_emitter}$ in advanced *npn* SiGe HBTs due to a lower doping density N_d in the C-B region, the capacitance in an inverse-switch's C-B region is much lower than the forward-switch's capacitance in the E-B region. In addition, smaller doping densities in the C-B region (as compared to the E-B region) of the diode-connected *npn* SiGe HBT Q1 corresponds to higher resistance in the path of the leaked signal when the switch is in the OFF state. Therefore, in the inverse-mode RF switch, a larger path resistance coupled with a smaller junction capacitance provides more impedance to the incoming RF signal, thereby improving isolation in the OFF state.

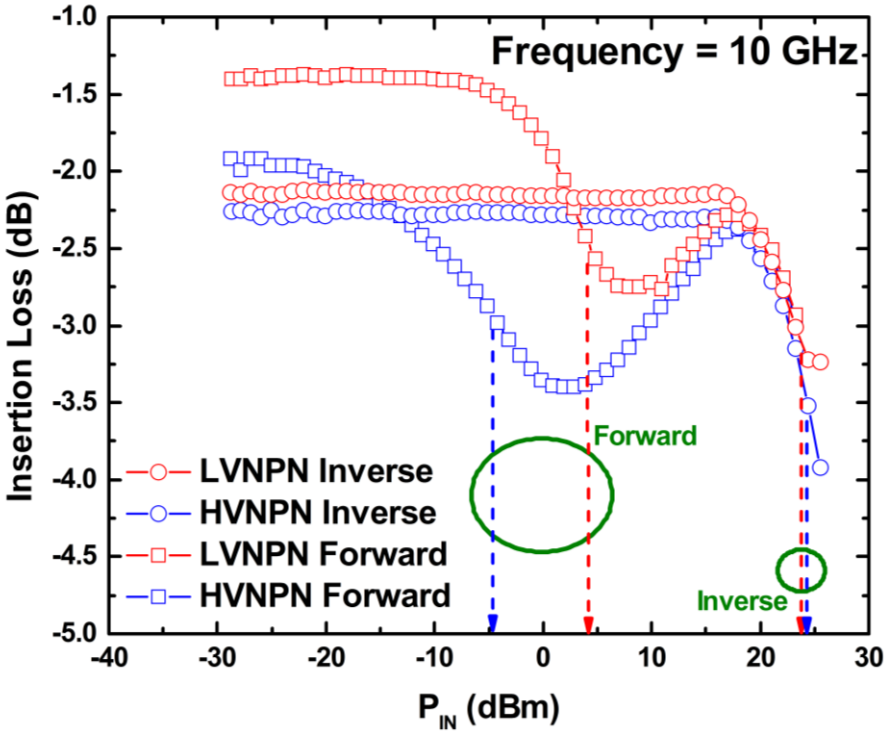

Figure 38: Measured ON state insertion loss of the forward- and inverse-mode RF switches under large-signal drive at 10 GHz. Onset of compression is marked with dashed arrows.

Figure 38 shows the variation in IL in the ON state at 10 GHz as the input continuous wave (CW) signal strength is increased (with 50 Ω input and output impedances maintained). With increasing RF input power, it can be observed that the forward-mode switches undergo a process of "dual-compression", where IL drops at around -10 dBm of input power, but then proceeds to increase (presumably due to self-biasing effects) before compressing again around +15 dBm input power. This effect is typically never reported for RF switches (it was seen only recently without explanation in [55]), thus making the concept of 1-dB compression point (P1dB) a fuzzy descriptor of large-signal saturation, a key metric for many RF switch applications. For both inverse-mode switches, P1dB occurs much later at around +24 dBm input RF power, just before the large *dc* currents start to induce electromigration. Therefore, if the "dual-

compression" phenomenon is ignored in forward-mode switches, it can be claimed that inverse-switches have an intrinsically much higher power handling capability, as shown in [56]. To make matters clearer, a better metric to judge RF switch compression characteristics could be the 3-dB compression point (P3dB), as is commonly used in the radar community.

3.2.3 Analysis

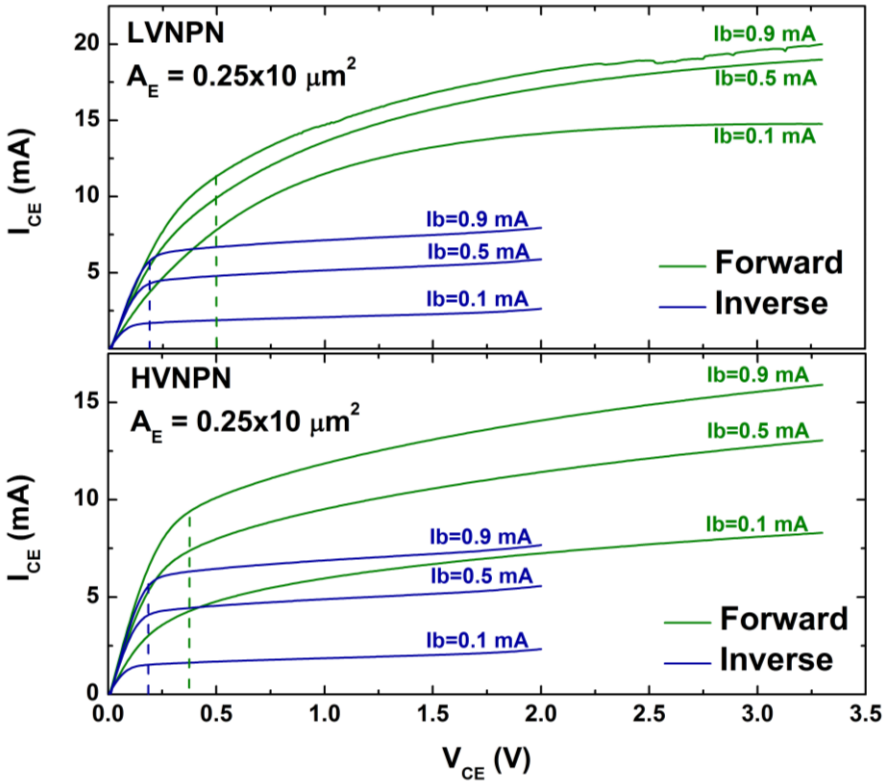

Figure 39: Output characteristics of the LV and HV npn SiGe HBTs in both forward- and inverse-mode of operation. The dashed lines represent V_{KNEE}, where the SiGe HBT transitions from the saturation region into the active region of operation.

An effective method of analyzing the measured switch results is to treat the switch as a lossy amplifier, where the switch IL is the equivalent of a negative amplifier gain. In Figure 39 the output characteristics of both the LV and HV *npn* SiGe HBTs are shown in the forward and inverse modes of operation. The dashed lines represent the

knee-voltage V_{KNEE}, where the SiGe HBT transitions from the saturation regime to the active regime. In the case of the diode-connected SiGe HBT in the ON path (Q1), $V_{CC} = V_{CE} = V_{BE} = \sim 0.85$ V. As described in [57], the location of the *dc* bias point in the I_C-V_{CE} plane significantly affects the maximum allowable swing. Signal compression occurs when the positive peak of the input signal rises above breakdown BV_{CEO} and the SiGe HBT enters the cutoff region, or the negative peak falls below V_{KNEE} and the SiGe HBT enters the saturation region. Since in a switch configuration where $V_{CE} = V_{BE} = \sim 0.85$ V and there is never a risk of breaching the upper "headroom" requirement for compression, the compression emanates from the proximity of the RF signal (superimposed on the *dc* bias point) to the saturation region by not having sufficient "legroom". The further the RF signal swing has to traverse to get to the saturation regime, the later the onset of compression will be. Therefore, smaller the voltage V_{KNEE}, the higher the switch P1dB will be. It can be seen from the output curves of the two transistors that the SiGe HBTs operating in forward-mode have a higher V_{KNEE} than that in the inverse-mode, thus providing a direct explanation of the results observed in Figure 38.

According to [58], V_{KNEE} can be written as :

$$V_{KNEE} \propto \ln\left(\frac{1+(\beta_{sat}+1)/\beta_{inv}}{1-\left(\frac{\beta_{sat}}{\beta_{fwd}}\right)}\right), \tag{12}$$

where β_{sat}, β_{fwd}, and β_{inv} are the *dc* current gains in the saturation, forward, and inverse modes of operation, respectively. Thus by careful optimization of the germanium profile in the SiGe HBT [11], V_{KNEE} can be tuned to yield high-performance SiGe HBTs capable of very high RF power handling capabilities.

3.2.4 Summary and Implications

In this section, the data and analysis for understanding the differences in forward-mode vs. inverse-mode operation of SiGe HBTs in the context of high-power RF switches was presented. Key takeaways include:

1. Everything else being equal (*dc* power dissipation, SiGe HBT geometry, etc.), inverse-switches show similar insertion losses as forward-switches in the ON-state of operation.
2. Everything else being equal, inverse-switches have equal or better OFF-state isolation compared to forward-mode switches.
3. Inverse-mode switches have better power-handling capability and compression characteristics than forward-mode switches.
4. The tuning knob to control SiGe HBT switch linearity is V_{KNEE}, which can be optimizing by varying the Ge profile and doping densities.

3.3 Addressing Noise Floor Concerns

3.3.1 Minimizing Crosstalk in High-Resistivity Substrates

Noise floor brings up the rear-end of the dynamic range spectrum. Noise floor can either be thermally modulated (with increasing ambient temperatures, noise floor tends to rise) or it can be affected by the presence of other noise creating circuits such as fast digital circuit blocks nearby. From the perspective of mixed-signal system-on-chip (SoC) designs with both RF/analog and digital components, SOI technology is extremely advantageous since the insulating nature of the substrate can improve RF noise isolation between the digital and RF/analog components [59]. For instance, in a bulk silicon substrate, high-frequency switching in the clock-trees of the SoC leads to the injection of undesirable transients into the silicon substrate, which can perturb transistor performance in the RF/analog sub-blocks of the SoC. This noise injected into the substrate by clock trees or even by RF voltage controlled oscillators [60], is referred to as crosstalk noise, or simply crosstalk. In the context of wireless communications, crosstalk noise is highly detrimental since it works to effectively raise the noise floor of the system , thereby deteriorating the dynamic range of a communication system (e.g. transceiver). As a

result, the weakest signals become undetectable by the wireless system. Due to their insulating substrates, SOI technologies help to mitigate crosstalk noise in a chip. In addition, particularly when a thick-film insulator and high-resistivity silicon substrate is used, the substrate losses are greatly reduced. The reduction of substrate losses also enables fully integrated on-chip passives such as inductors and capacitors with very high quality-factors [61].

A large database of literature exists on methods to model and minimize crosstalk in mixed-signal ICs fabricated on silicon substrates. In the excellent work by K. Joardar [62], crosstalk reduction using SOI and guard rings was studied and crosstalk performance was modeled using the SPICE simulation program. In [63], a lumped-element equivalent circuit of crosstalk propagation was introduced, and this work confirms those results. The use of on-chip metal Faraday cages to minimize crosstalk was explored in [64]. More recently, [65] investigated substrate crosstalk in both standard and trap-rich high-resistivity silicon substrates. However, to date, no study has been performed on the effectiveness of using concentric rings of deep trenches (DT) around a sensitive RF/analog circuit to reduce crosstalk noise between sensitive circuit blocks. Deep trenches are highly insulating by design, and no additional masks have to be used to deploy them as noise shields, unlike the buried metal ground method in [64]. This is the first study to address the feasibility of using DTs as a crosstalk mitigating mechanism in mixed-signal SoCs.

There is a dearth of literature on the effect of cryogenic temperatures on crosstalk, and its implications for high dynamic-range cryogenic circuits. Due to their band-gap engineered nature [11], SiGe technologies are the perfect enabler of high-performance and reliable cryogenic circuit design. Recently, the feasibility of using SiGe technologies for cryogenic RF circuit design was demonstrated in [66, 67, 5, 68], and the integration of cryogenic RF circuits with SiGe based digital blocks for extreme environment applications [69] is gathering significant interest. For such high dynamic-range systems,

crosstalk at cryogenic temperatures will be a major with which issue to contend.

The BiCMOS process used in this work [16] uses a thick-film SOI (0.1 μm) for isolation between digital and RF/analog circuits, as well as a high-resistivity (~1K Ω–cm) silicon substrate to enable passives with very high Q-factors. Therefore, the process in [16] is ideal for high-performance RF system design. This work lays the foundation for studying how crosstalk noise can cause circuit performance variation (with a focus on reduction in dynamic range) as a function of changing ambient temperatures in high-resistivity thick-film SOI substrates.

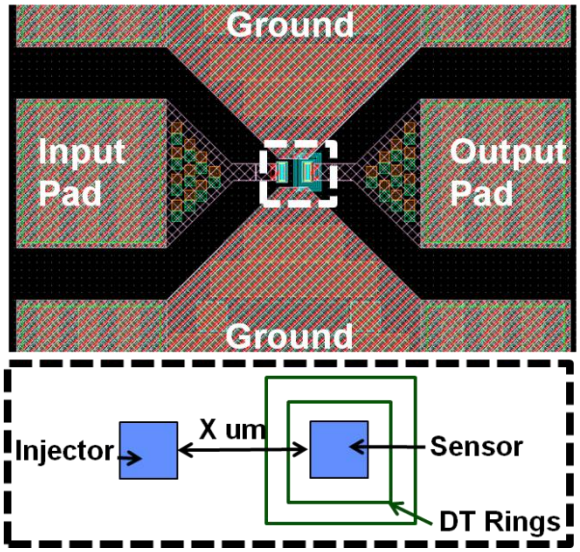

Figure 40: Layout of the crosstalk test structure, with a top-view of the outlined part magnified below.

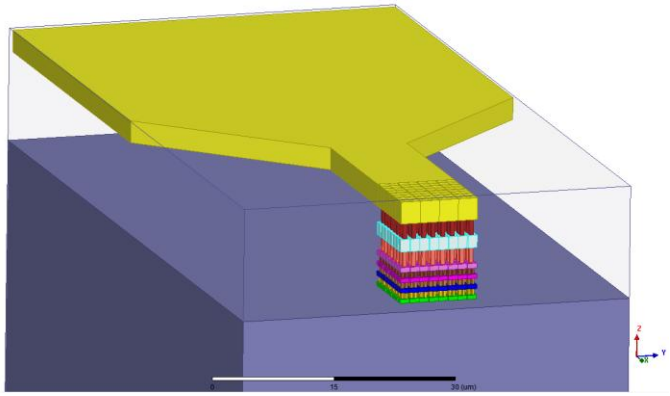

Figure 41: A 3-D rendering of the interconnects between the signal pad and the noise-injector/sensor HBT.

3.3.2 Hardware Description and Measured Results

A. Hardware Description

A detailed pictorial representation of the crosstalk structures is shown in Figures 41 and 42. Ground-Signal-Ground (GSG) RF pads at the input were connected to the collector of a high-performance *npn* SiGe HBT with a selectively implanted collector [16]. This HBT acted to inject RF noise into the high-resistivity silicon substrate through the buried oxide (BOX), and is hence termed as the "noise-injector" or injector. A similar second high-performance *npn* SiGe HBT was placed a set distance away from the noise-injector, with its collector connected to the output GSG RF pads. This second HBT acted to sense the noise in the substrate though the BOX, and is hence termed as the "noise-sensor". A set of input and output GSG pads, noise-injector, and noise-sensor constituted one crosstalk measurement structure. As depicted by 'X' μm in Figure 40, the crosstalk structures had increasing separations (1, 5, 10, or 20 μm) between the injector and the sensor. In addition, the noise-sensor was surrounded by 0, 1, 2, or 3 deep trenches (in addition to one deep trench that was inherent to every *npn* SiGe HBT p-cell layout). The buried oxide was 145 nm thick, and the underlying substrate had a very high resistivity (around 1K Ω–cm). In this work, two methods of minimizing crosstalk noise were analyzed: isolation by increasing distance and isolation by increasing concentric DTs.

B. Measured Results

Since there is no signal amplification in an all-passive, highly attenuative crosstalk structure, integrity of the sensed RF signal can become questionable. For this reason, special measures have to be taken to ensure that the measurement test-bench has a high dynamic range. For all measured results presented in this work, S-parameter measurements were performed with an unusually high source power of -10 dBm. To ensure extreme stability of measured data, the measured S-parameter results were averaged eight times. In addition, to dramatically lower the noise floor of the network analyzer, the Intermediate Frequency (IF) filter was set to 50 Hz.

The parameter S_{21} was chosen as the metric to quantify crosstalk; higher S_{21} translates into a worse crosstalk performance as it corresponds to higher RF signal levels being sensed at the output port. All S_{21} results shown are taken from raw measured S-parameters; the pads have not been de-embedded from the measurements using traditional methods such as Open-Short/TRL. This translates into higher crosstalk across all frequencies for all structures. The reason for presenting measured results in this way stems from the fact that de-embedding is an approximation that only works best when the parasitics (and associated losses) introduced by the metallization of the test-structure are much smaller than the parasitics (and associated losses) native to the intrinsic Device Under Test (DUT). For this reason itself, the smallest sized transistor is the most difficult one to reliably measure and de-embed. A crosstalk structure is intrinsically very lossy due to the absence of active devices and also riddled with RLC parasitics. Therefore, reporting raw S-parameters is not uncommon for crosstalk measurements [70].

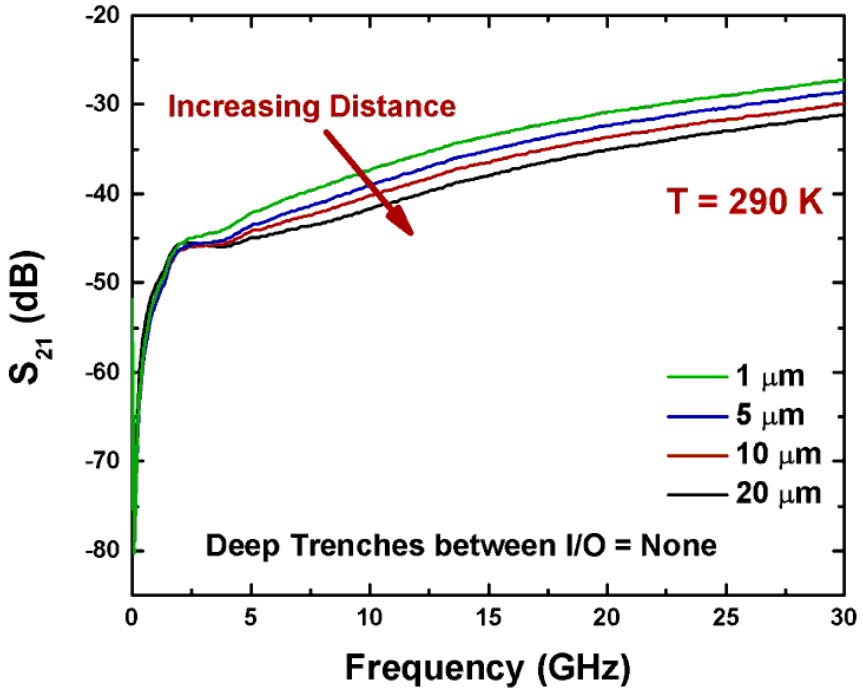

Figure 42: Room temperature crosstalk performance for structures with increasing physical separation between noise-injector and noise-sensor.

The measured crosstalk performance at room temperature for four crosstalk

structures with increasing physical distance (1, 5, 10, and 20 µm) between the noise-injector and noise-sensor is shown in Figure 42. For all the structures in Figure 42, there were no additional DTs encircling the noise-sensor. At very low frequencies (< 1 GHz) where crosstalk is not a major concern, all four structures display the same results. At higher frequencies, a greater distance between the noise-injector and sensor results in a monotonic improvement in crosstalk performance. With the fastest SiGe analog-to-digital converters (ADC) currently operating at speeds as high as 50-GS/s [71], it follows that to ensure sufficient isolation at higher frequencies, the RF/analog circuit blocks should be spaced as far away from the fast digital blocks as possible. For example, moving a mere 20 µm from the noise-injector helps to reduce the crosstalk by more than half (4 dB decrease at 7.5 GHz).

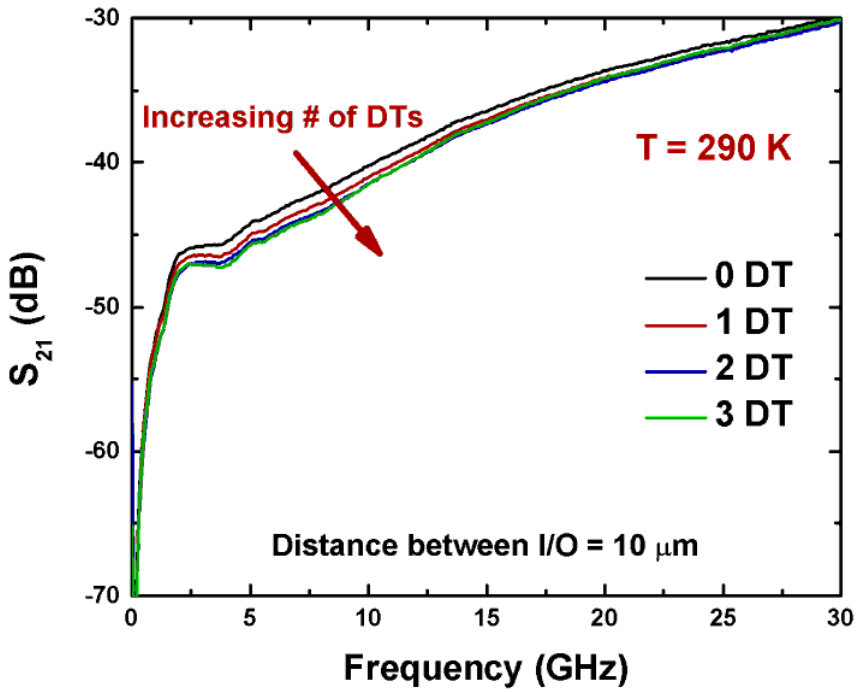

Figure 43: Room temperature crosstalk performance for structures with increasing number of deep trenches between noise-injector and noise-sensor.

The crosstalk measurement results at room temperature of test-structures with increasing number of DTs (0, 1, 2 and 3) encircling the noise-sensor are shown in Figure 43. The DTs, used to define CMOS junction isolation regions, are patterned and filled

with oxide which has a very low dielectric constant, as well as polysilicon to relieve the stress. These DTs are placed in addition to the default DT that encircles both the injector and the sensor HBT as a part of their layout p-cells. The distance between the injector and the sensor was fixed to be 10 µm in all four structures. As shown in Figure 43, the improvement obtained in crosstalk performance from placing an additional DT around the sensor (going from 0 to 1 DT) is minimal; around 0.8 dB at 7.5 GHz. Putting additional DTs around the sensor does not work to further improve crosstalk isolation. This leads to the conclusion that using concentric DTs for minimizing crosstalk in a mixed-signal chip is not a very effective mechanism for isolating sensitive RF/analog circuits from noisy digital blocks, and increasing the physical distance between sensitive blocks is still the preferred strategy.

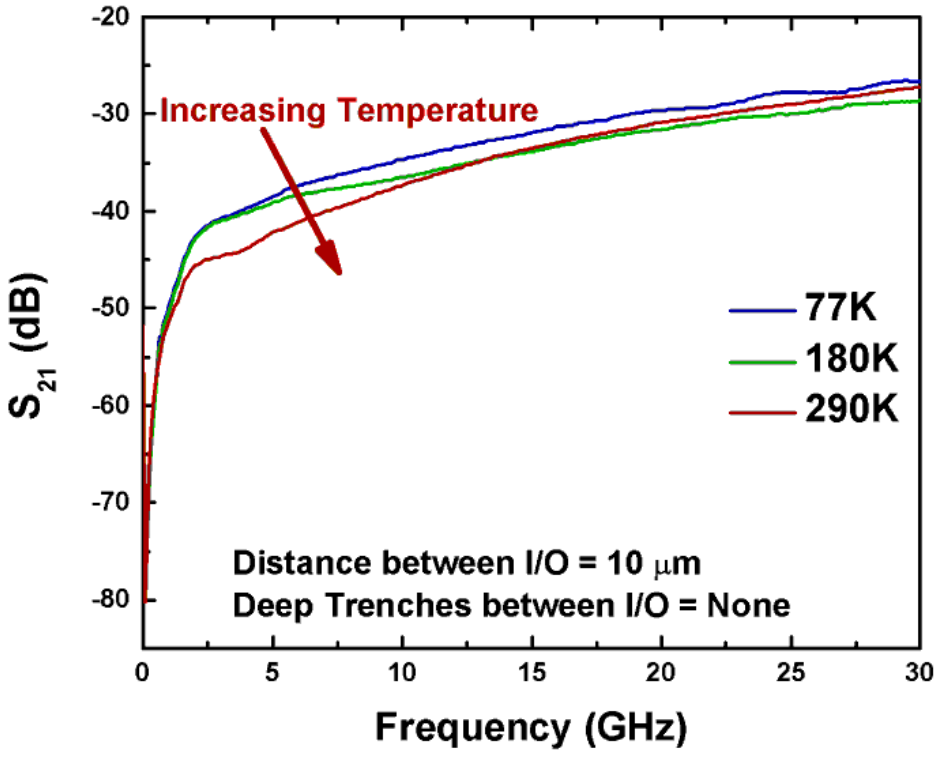

Figure 44: Crosstalk performance across temperature for a structure with noise-injector and noise-source 10 µm apart, and no additional DT.

Figure 44 shows the crosstalk in a test-structure (with the noise-injector and

sensor 10 µm apart) with varying ambient temperatures. In these structures there is no additional DT encircling the sensor. Up to very a high frequency (around 15 GHz), the crosstalk noise follows a monotonic trend with temperature – as temperature increases, the crosstalk injection through the substrate reduces. At very high frequencies, the losses become increasingly distributive, leading to deviations from the observed trends. The results in Figure 44 indicate that the dynamic range of cryogenic mixed-signal circuits can be affected with changing ambient temperatures, an issue that needs to be explicitly addressed by mixed-signal circuit designers.

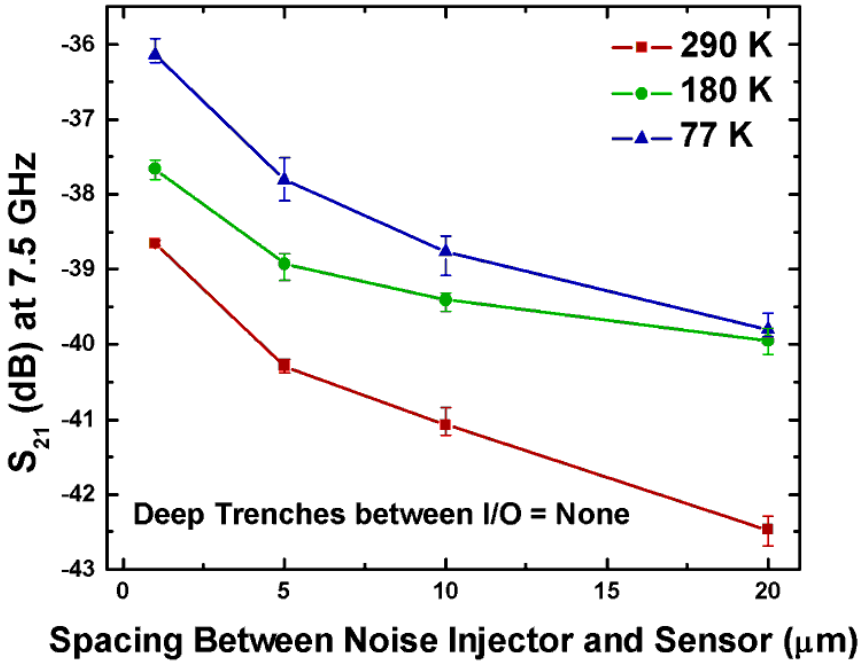

Figure 45: Mean value of measured crosstalk with +/- error bars for increasing distance between noise-injector and sensor with varying temperature.

To extricate clarity from all measurements taken from multiple silicon wafers at different temperature points, y-axis error bars are employed in Figure 45 and Figure 46. The measured S_{21} is shown at a fixed frequency of 7.5 GHz across a very wide range of temperatures (greater than 200 K). Figure 45 shows the effect of increasing the distance between noise-injector and sensor at 290 K, 180 K, and 77 K. It is seen that crosstalk has a clear dependence on both ambient temperature, as well as distance between injector and

sensor. The difference in crosstalk performance from 1 μm spacing to 20 μm spacing is significant (around 4 dB at 290 K). It is also observed that the crosstalk for a given separation between the injector and the sensor increases with decreasing temperature. This is explained in detail in Section 3.3.3.

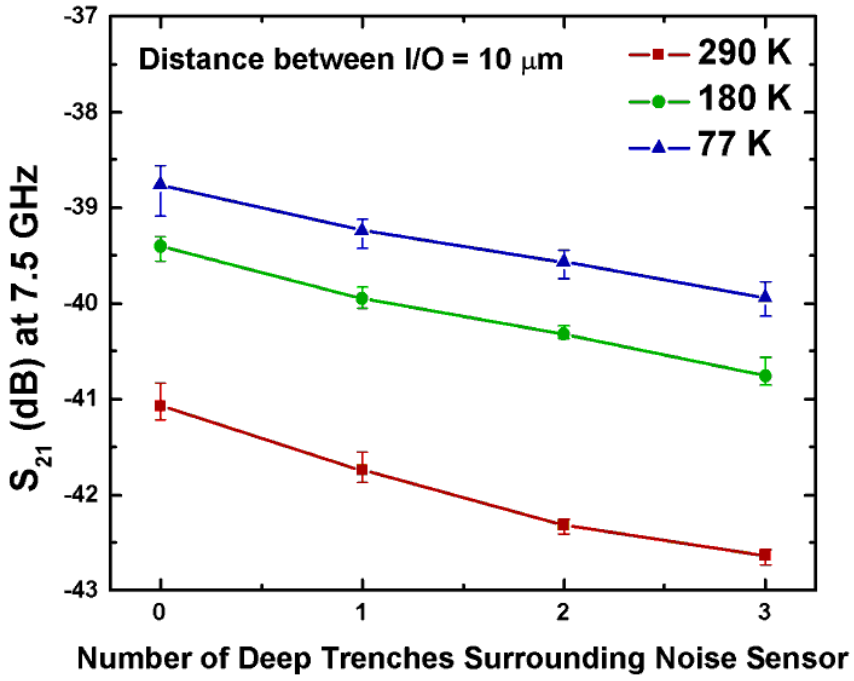

Figure 46: Mean value of measured crosstalk with +/- error bars for increasing number of deep trenches between noise-injector and sensor with varying temperature.

Figure 46 shows the effect of increasing the number of DTs around the noise-sensor on crosstalk with varying ambient temperature. While additional DTs encircling the sensor do seem to mitigate crosstalk, it is apparent that this is a much weaker mechanism than physically separating the injector and the sensor (as in Figure 45). For example, at 77 K, the attenuation achieved in crosstalk by going from no DT to 3 DTs encircling the sensor is only approximately 1.2 dB. Thus, using additional DTs for the sole purpose of crosstalk mitigation is not desirable.

3.3.3 Analysis

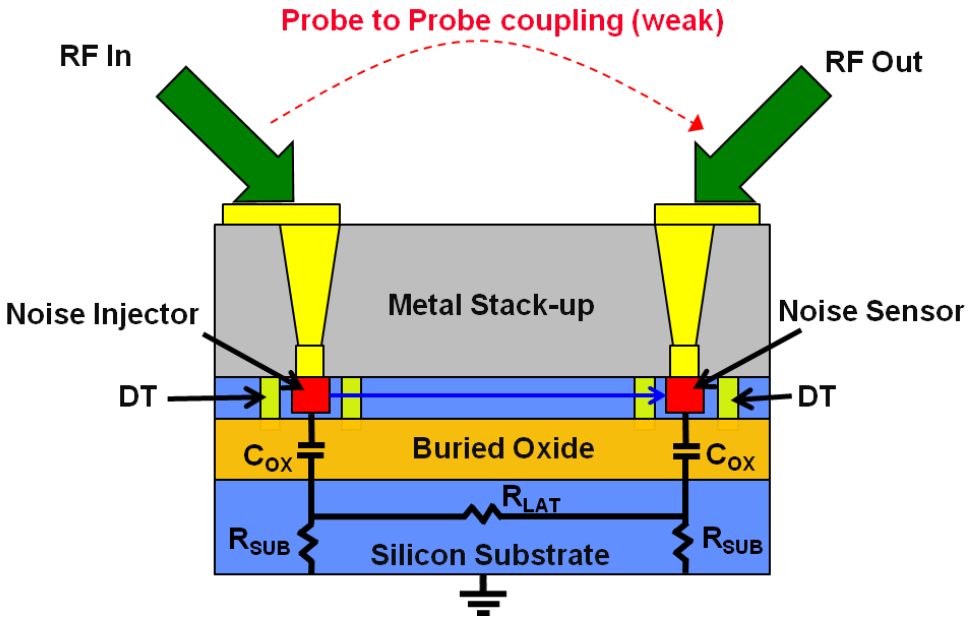

Figure 47: Block-diagram of the crosstalk test structure showing various mechanisms of signal leakage from input probe to output probe.

A block-diagram of the test structure cross-section is shown in Figure 47. Three anticipated mechanisms of signal transfer from input probe to output probe in a crosstalk measurement are (in decreasing order of magnitude) – signal coupling through the buried oxide and high-resistivity silicon substrate of the SOI handle wafer (strongest), signal transmission through highly doped silicon and patterned DTs above the buried oxide (weak, depicted by the blue arrow going from noise-injector to sensor), and RF probe-to-probe coupling (very weak, depicted by the red dashed arrow). The lumped component C_{OX} denotes the capacitance formed between the n^+ silicon above the BOX and the high-resistivity silicon substrate underneath it; R_{LAT} denotes the resistance of the lateral conduction path in the high-resistivity substrate; R_{SUB} denotes the resistance between the substrate and ground [63].

The transfer function of the equivalent lumped-element circuit in Figure 7 is given

by:

$$\frac{V_{sensor}}{V_{injector}} = \frac{j * w * C_{OX} * {R_{SUB}}^2}{2R_{SUB} + R_{LAT}(j * w * C_{OX} * R_{SUB} + 1) + j * w * C_{OX} * {R_{SUB}}^2}. \quad (13)$$

The lateral signal resistance R_{LAT} is determined by the equation:

$$R_{LAT} \propto \rho_{SUB} * L_{SI}, \quad (14)$$

where ρ_{SUB} is the substrate resistivity (~1K Ω-cm at room temperature), and L_{SI} is the distance between the sensor and the injector. With increasing L_{SI}, as in Figure 42, R_{LAT} increases monotonically. Since R_{LAT} appears in the denominator of the transfer function, the overall transfer function of the signal transmission reduces with increasing R_{LAT}. Thus with increasing distance, the RF signal attenuates, leading to decreased S_{21} and improved crosstalk.

In the equivalent lumped-element model circuit, the signal leakage through n+ silicon and DTs is not accounted for, since it is not a dominant mechanism of crosstalk. A very detailed equivalent circuit model for a deep trench is discussed in [72]. To simplify the analysis, if we neglect the charge perturbations within the polysilicon layer due to recombination and generation processes, a deep trench can be reduced to merely a capacitor filled with a low-κ dielectric. The very small capacitance value hinders the RF signal from propagating through it, leading to good isolation across its terminals. Since each noise-injector and sensor HBT has a DT built into its p-cell, adding additional DTs does not significantly help in minimizing crosstalk.

To understand why crosstalk is a function of temperature, the variation in properties of high-resistivity silicon as a function of temperature needs to be analyzed. The seminal work on modeling the mobility of carriers in silicon by D. B. M. Klaasen as a function of doping densities was presented in [73], and as a function of changing temperatures presented in [74]. The mobility model in these companion papers accounts

for not only the donor, acceptor, and lattice scattering, but also electron-hole scattering, clustering of impurities, and impurity screening by charge carriers. The model lends itself easily to this study because it provides the carrier mobility as a function of donor, acceptor, electron, and hole concentrations. From [73-75], the temperature dependence of the lattice scattering mobility is captured by the well-known power-law equation:

$$\mu_{e,Lattice} = \mu_{max}\left(\frac{300}{T}\right)^{\theta_e}, \tag{15}$$

where μ_{max} is the maximum achievable mobility for a given dopant under very low doping concentrations, and θ_e is an empirical fitting parameter. In a similar way, the impurity scattering mobility value of the majority carrier depends upon both doping concentration and temperature, and is expressed as

$$\mu_{e,D}(N_D, c) = \mu_{e,N}\left[\frac{N_{ref,1}}{N_D}\right]^{\alpha_1} + \mu_{e,c}\left(\frac{c}{N_D}\right). \tag{16}$$

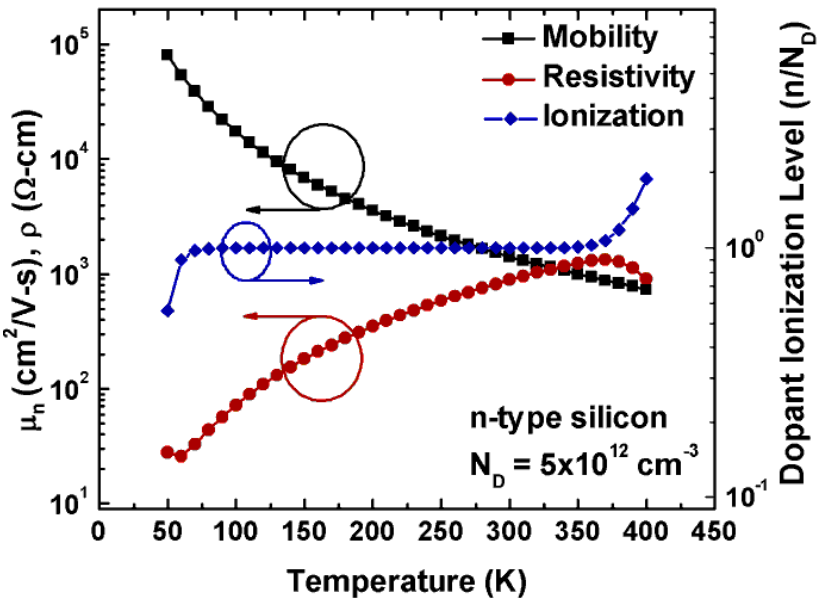

Figure 48: Mobility and resistivity of the high-resistivity silicon substrate as a function of varying temperatures.

The resistivity of the silicon substrate used in this work [16] is very high, approximately

1K Ω–cm at room temperature. This translates into an n-type (Arsenic) doping concentration of roughly $5x10^{12}$ cm^{-3}. Using this doping concentration as an input parameter for Klaasen's mobility models, the mobility of the majority n-type carrier, as well as resistivity of the silicon substrate, is calculated for varying temperatures (as in [75]). The results are shown in Figure 48. As expected, we observed that for a high-resistivity silicon substrate, the resistivity decreases considerably with decreasing temperature. This phenomenon is explained very well in [74, 75], where it was shown that the lattice scattering mobility dominates the temperature dependence of the carrier mobility for silicon substrates with lower doping concentrations. Lattice scattering reduces with decreasing temperatures, resulting in a higher carrier mobility and lower resistivity.

The outcome of decreasing substrate resistivity and increasing carrier mobility is that the substrate becomes more conductive as the ambient temperature decreases. From equation 14, we see that the value of R_{LAT} decreases with temperature, and when this result is applied to equation 13, it becomes apparent as to why reducing temperatures leads to worse crosstalk performance. The dopant ionization levels are also shown in Figure 48, which shows that incomplete ionization does not occur in the temperature ranges used in this study.

3.3.4 Summary

A detailed investigation of crosstalk noise in high-resistivity thick-film SOI substrates has been presented. Two methods of crosstalk mitigation have been studied: isolation by increasing distance and by increasing concentric deep trenches around sensitive RF/analog circuits. Furthermore, for the first time, the dependence of crosstalk on ambient temperature has been studied. The key takeaways of this work are:

1. Increasing the distance between a noise-injecting circuit such as digital clock-trees and a sensitive RF/analog circuit is the best (and the easiest) method to attenuate crosstalk noise.
2. Increasing the number of concentric deep trenches around a sensitive RF/analog circuit definitely helps to mitigate crosstalk, but is a much weaker mechanism than the one described above.
3. For high-resistivity substrates, decreasing the ambient temperature leads to higher carrier mobility, and therefore lower substrate resistivity. This makes the substrate more transparent to RF/microwave signals, and thus crosstalk increases.

3.4 Addressing Compact Model Concerns

3.4.1 Motivation

In order to design high-performance circuits with a first-pass success, it is absolutely mandatory for the compact models used during the design phase to capture all parameters (*dc*, *ac*, RF) with a very high degree of fidelity. The conventional compact model fitting process aims to fit the models only to measured *dc*, *ac*, and 1/f noise data for a given temperature, because only the data from these measurements forms the input of the compact model's parameter extraction process. There are no measurement-to-model overlays generated for advanced RF parameters such intermodulation (IIP3),

broadband noise (noise-figure), or gain-compression (P1dB). For estimation of these parameters, the circuit designers have no reliable go-to method, and must have faith in the model's ability to predict these higher-order effects. For SiGe HBTs, there exist many compact models for the designers to rely upon, e.g. VBIC [49], HICUM [50], MEXTRAM. The question that most designers find themselves asking is: which compact model to rely on to predict not just the *dc* and *ac* parameters, but also higher-order RF effects such as third-order (IMD3) and fifth-order (IMD5) intermodulation, and gain-compression.

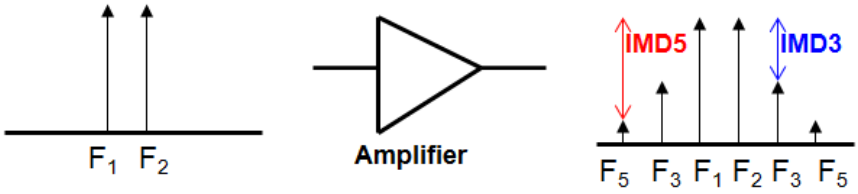

Figure 49: Harmonic generation at the output of an amplifier with two input tones, f_1 and f_2.

To reiterate, Figure 49 illustrates an amplifier with two input frequencies f_1 and f_2, and the generation of third-order intermodulation terms (F_3) at frequencies $2f_2$-f_1, $2f_1$-f_2, and fifth-order intermodulation terms (F_5) at frequencies $3f_1$-$2f_2$ and $3f_2$-$2f_1$. All of these frequencies lie very close to desired fundamental tones, f_1 and f_2, thus making rejection by filtering impossible. Unfortunately, modeling these harmonic-generation effects in a CAD environment is a very complex problem, and no clear answer presently exists on which bipolar compact model best predicts these trends accurately. This work answers the question of which compact model is preferred in the context of C-SiGe platforms by comparing HICUM [50] and VBIC [49] compact models for the *pnp* SiGe HBT in a leading-edge C-SiGe on SOI platform. Recent studies [1, 76] on such C-SiGe platforms

have shown that the pnp SiGe HBTs have superior RF performance over their *npn* counterparts in terms of power gain and RF linearity, opening up a realm of interesting design possibilities in high-linearity analog/RF circuit design.

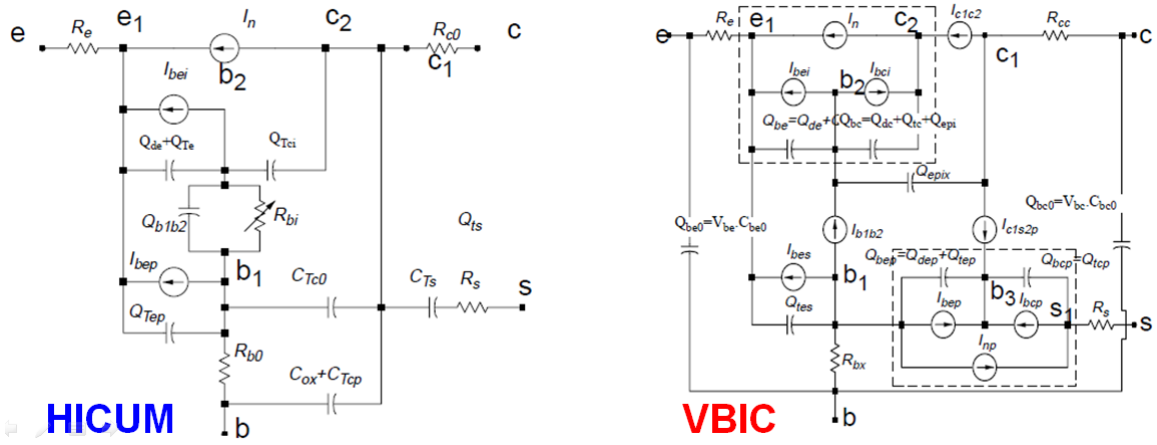

Figure 50: Equivalent Circuits of the HICUM and VBIC Compact models.

Figure 50 shows the simple equivalent circuits of both the HICUM and the VBIC compact models. HICUM stands for "HI CUrrent Model", while the VBIC expands to "Vertical Bipolar Intercompany Model". As a comparison, the HICUM has 5 internal nodes, and the VBIC has 7 internal nodes. A compact model with fewer numbers of internal nodes will be inherently simpler in its mathematical formulations, and will also have an increased probability of converging properly during a simulation. In addition, the HICUM model has 101 modeling parameters as compared to 108 parameters within the VBIC model. Again, fewer modeling parameters correspond to simpler compact model formulations. The version of the HICUM model used in this work is "HICUM Level0".

3.4.2 Experimental Details

The *dc*, *ac*, and RF linearity characteristics of the *pnp* SiGe HBTs at room

temperature (300 K) were measured. The input and output impedances of the DUT were fixed at 50 Ω to ensure repeatable test conditions across three test sites. The *pnp* SiGe HBTs were connected to G-S-G pad configuration, and were 0.25x10 μm^2 in geometry.

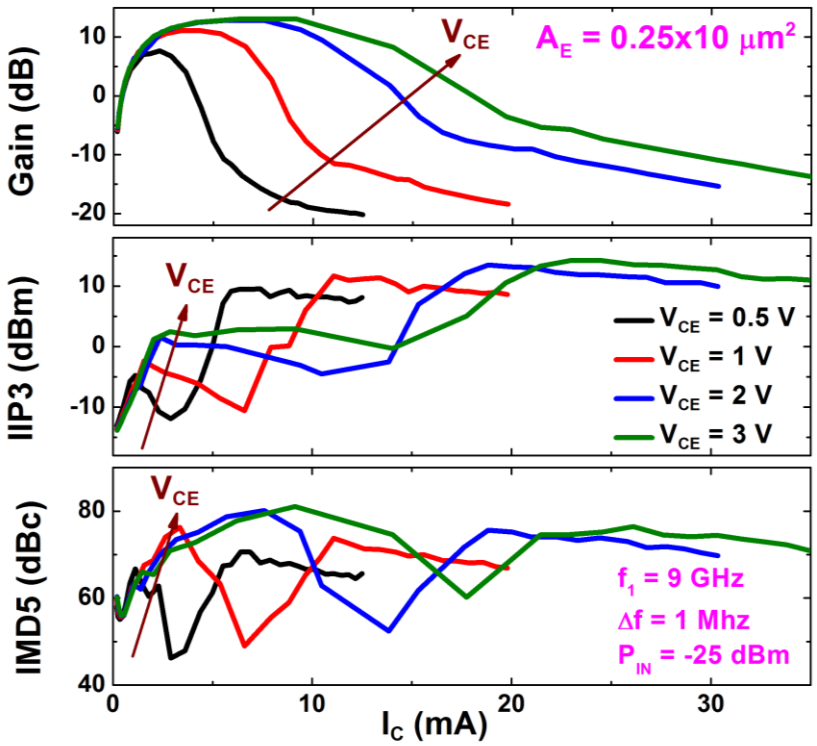

Figure 51: Measured RF data of the pnp SiGe HBT.

Input continuous wave (CW) tones of 9.000 GHz and 9.001 GHz were applied to the DUT at varying *dc* bias conditions. The power of the input tones was set to be in the small-signal regime, and was -25 dBm (35.56 mV peak-to-peak at 50 Ω) for our experiment. Measured RF results are shown in Figure 51. It is clear that the RF data obtained is very clean, and follows trends predicted by theory. For example, with increasing V_{CE}, C_{CB} capacitances become more linear and hence the SiGe HBT IIP3 increases (this was also observed in [1]).

Both the HICUM and VBIC models in this process design kit (PDK) have 5 corner models each for the *pnp* SiGe HBT (*C1*-*C5*). To ensure that the most representative corner model was used for verification of measured RF data, *dc* and *ac* data were measured on the *pnp* SiGe HBT and overlaid against data from Spectre corner simulations.

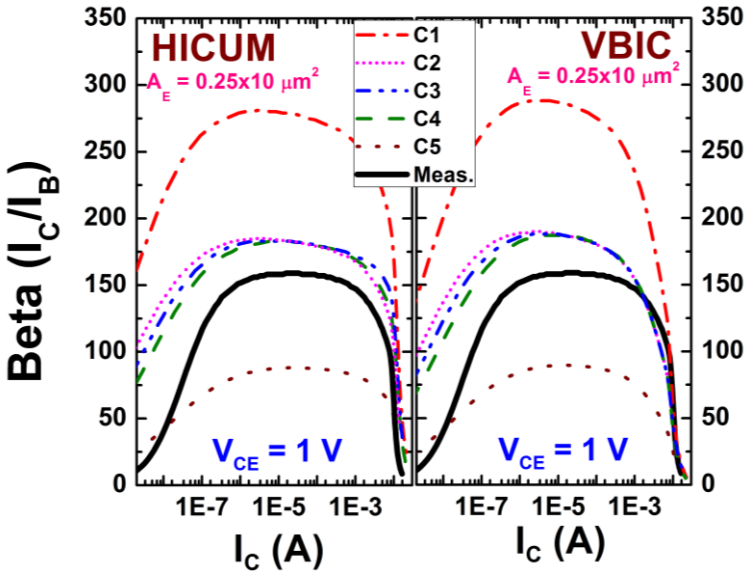

Figure 52: Current gain as a function of I_C for all HICUM (left) and VBIC (right) corner models. Models C1 and C5 do not predict measured dc trends of the pnp SiGe HBT.

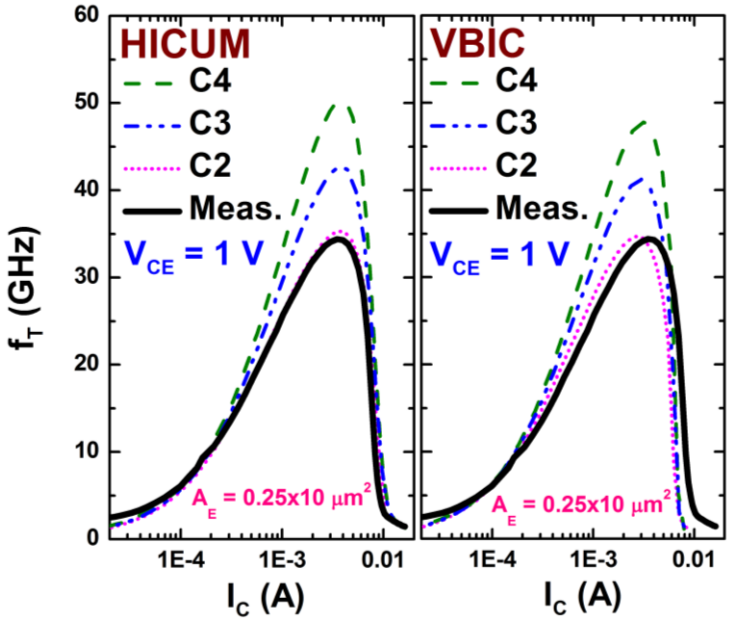

Figure 53: Cutoff frequency as a function of I_C for various HICUM (left) and VBIC (right) corner models. C2 is the correct corner model for both HICUM and VBIC.

It is apparent from Figure 52 that corner models *C1* and *C5* (for both HICUM and VBIC models) do not reflect measured current gain (β) trends of the silicon used in this work. This narrows down our choice to the remaining three corner models (*C2*, *C3*, and *C4*), which best represents our data. Figure 53 shows the overlay of measured and modeled *ac* data of the *pnp* SiGe HBT. The pad and interconnect parasitics were carefully de-embedded using standard OPEN and SHORT structures. Since the measured *dc* and *ac* characteristics of the HBT align well with the *C2* corner model for both the HICUM and the VBIC compact models, it was selected for validation of the measured RF data. For all simulation purposes (*dc*, *ac*, RF), SiGe HBT self-heating effects were enabled, since the *pnp* SiGe HBTs are fabricated on thick film SOI, where self-heating is a significant concern [77].

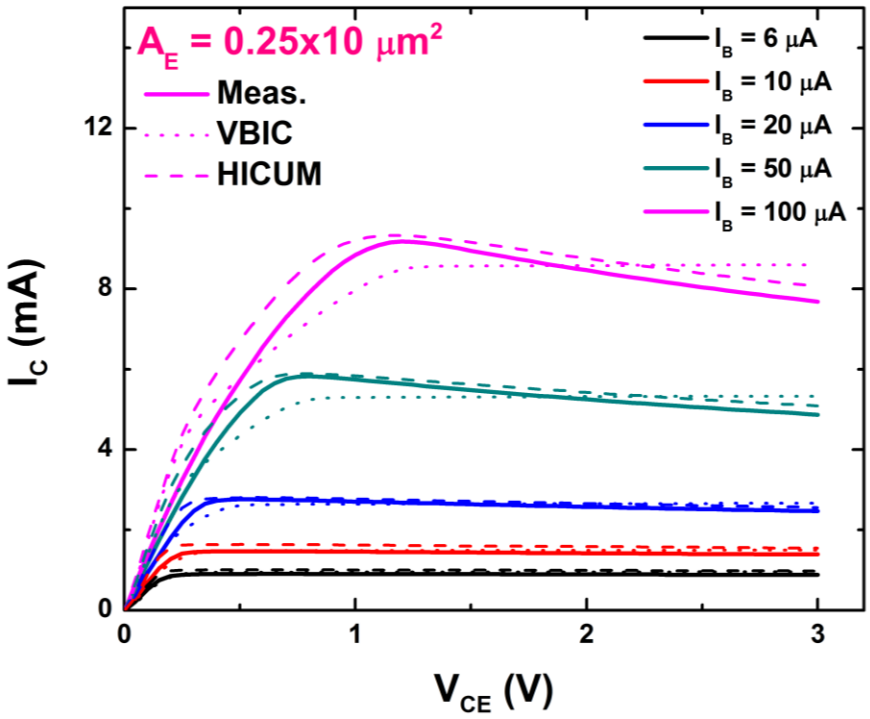

Figure 54: Comparison of measured output characteristics (solid) with HICUM (dashed) and VBIC (dotted) for various base currents.

Using the selected corner models (*C2*), simulated output characteristics of the *pnp* SiGe HBT were compared against measured data (Figure 54). The HICUM model gives good agreement with measured results, due to differences between how HICUM and VBIC implement their physics. HICUM's charge-based approach incorporates bias-dependent effects such as transit time, Early effect, and current-crowding at high currents in a singular physical formulation, the absolute charge Q_{PT}.

In addition, quasi-saturation is very efficiently formulated in HICUM. VBIC, in contrast, relies on a modified Kull approach to model quasi-saturation effects [78]. The Kull model, however, is valid for ohmic quasi-saturation only, when the carrier drift velocity is linearly proportional to the electric field. This is the case for only very low I_B (or V_{BE}) *dc* bias points [79], which the VBIC appears to predict quite well. At high I_B (or V_{BE}) scenarios, however, current crowding effects can dominate *dc* characteristics, which

HICUM effectively models due to its current- and voltage-dependent forward transit time (T_{FT}) parameter. This enables the HICUM model to better predict the output characteristics of the *pnp* SiGe HBT over a broader range of base currents.

3.4.3 Analysis

Modeling RF intermodulation involves, at its simplest, taking higher order derivatives of the static *I(V)* and *Q(V)* functions to calculate node voltages and currents. For instance, modeling third-order intermodulation (IIP3) and fifth-order intermodulation (IMD5) requires that third- and fifth-order derivatives of above functions exist and be continuous [32]. Moreover, any combination of these derivatives must behave monotonically. This makes accurate modeling of RF intermodulation the most rigorous test of the accuracy for any compact model.

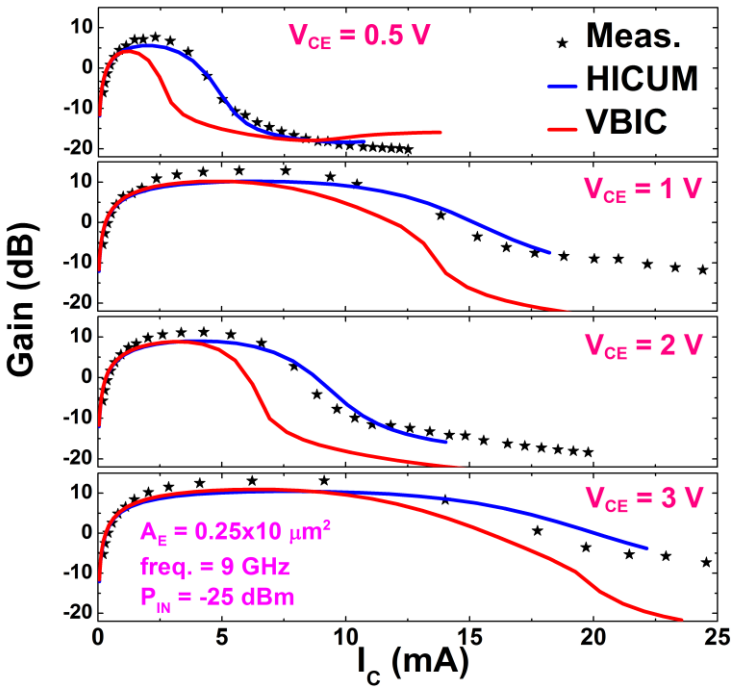

Figure 55: Comparison of measured and simulated power gain of the pnp SiGe HBT across varying collector voltages and currents.

Figure 55 shows the overlay of power gain of the *pnp* SiGe HBT as a function of collector current, for various *dc* collector biases. Due to its improved modeling of quasi-saturation effects, HICUM simulations accurately capture the measured gain, even at low V_{CE} values (e.g., 0.5 V). A robust power gain simulation is strongly dependent on the compact model's formulation of the SiGe HBT base resistance and internal capacitances, and must maintain convergence. To model the base resistance, VBIC uses a slightly modified version of the normalized base charge approach of the SPICE extended Gummel-Poon (SGP) model [80]. The disadvantage of this approach is that the output resistance of the SiGe HBT remains constant with changing *dc* bias. In HICUM, however, in addition to the current and voltage dependent total charge, parameters such as *QHEI* and *QJCI* take bias dependent base width modulation into account, and minority charge parameters such as *QF* model the effects of base conductivity modulation. All of these parameters, in addition to its improved quasi-saturation modeling, improve HICUM model's capabilities for accurately modeling the high-current region of operation

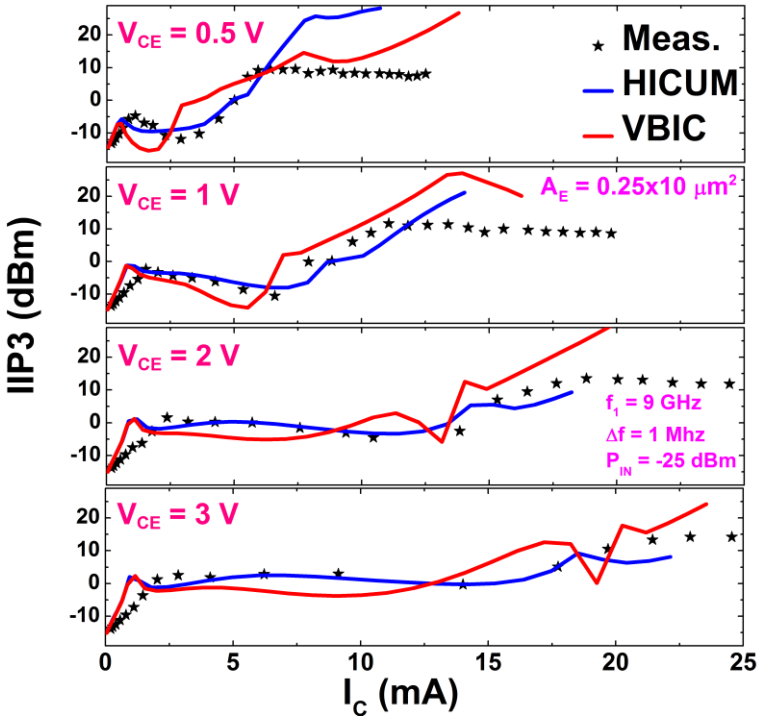

Figure 56: Comparison of measured and simulated IIP3 of the pnp SiGe HBT for varying collector voltages and currents.

Due to reasons such as bias dependent current, resistance and capacitance modeling in HICUM, HICUM models third-order intermodulation (IIP3) better than VBIC, as shown in Figure 56. The HICUM model, with its current dependent base-collector depletion capacitance modeling (a feature lacking in VBIC) predicts intermodulation more effectively. The greatest measurement-to-model discrepancy exists for regions with low V_{CE} and high I_C, where both models over-predict the IIP3 of the *pnp* SiGe HBT. This is due to the fact that at low V_{CE}, the base-collector junction is forward biased (weak saturation), and the resultant C_{CB} has both depletion and diffusion components to it. As V_{CE} increases, B-C junction becomes reverse-biased and C_{CB} becomes increasingly depleted. A depleted capacitance is easily modeled (and is also very linear) [28]. Thus as V_{CE} increases, so does the model accuracy for both HICUM

and VBIC models.

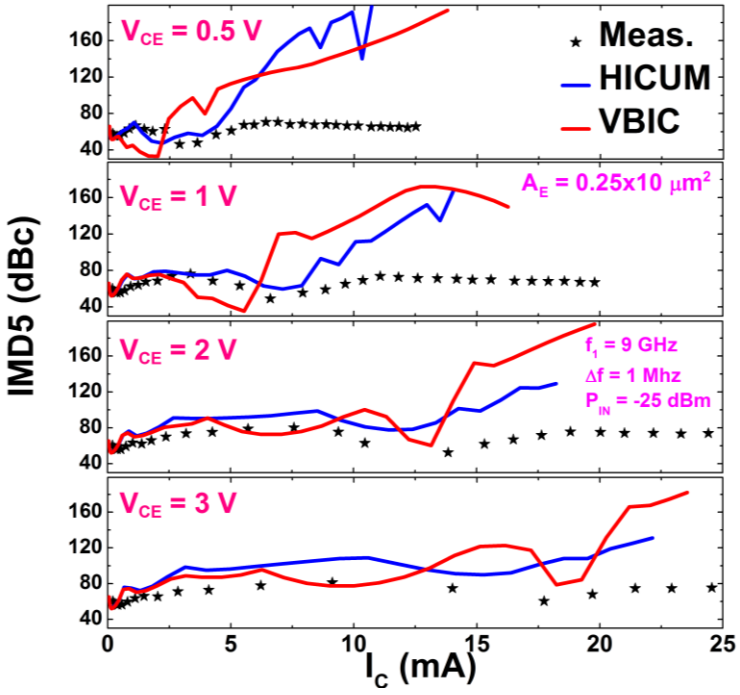

Figure 57: Comparison of measured and simulated IMD5 of the pnp SiGe HBT for varying collector voltages and currents.

As a final (stringent) test of the compact models' mathematical formulation and convergence robustness, measured IMD5 in dBc (positive difference of powers of fundamental-tone and fifth-order intermodulation tone) were also compared against simulation in Figure 57. Since the fundamental tones f_1 and f_2 are 9.000 GHz and 9.001 GHz, the fifth-order intermodulation terms are generated at $3f_1$-$2f_2$ and $3f_2$-$2f_1$ (i.e., 8.998 GHz and 9.003 GHz). IMD5 is a critical design parameter for overdriven RF power amplifiers. Typically, such circuits are operated with the active SiGe HBT cores biased close to the breakdown voltage (very high applied V_{CE} is needed to get maximum output power and power gain). For such scenarios (high V_{CE} and high I_C), the compact models are at their best at predicting IMD5, with HICUM simulations much closer to measured data than VBIC.

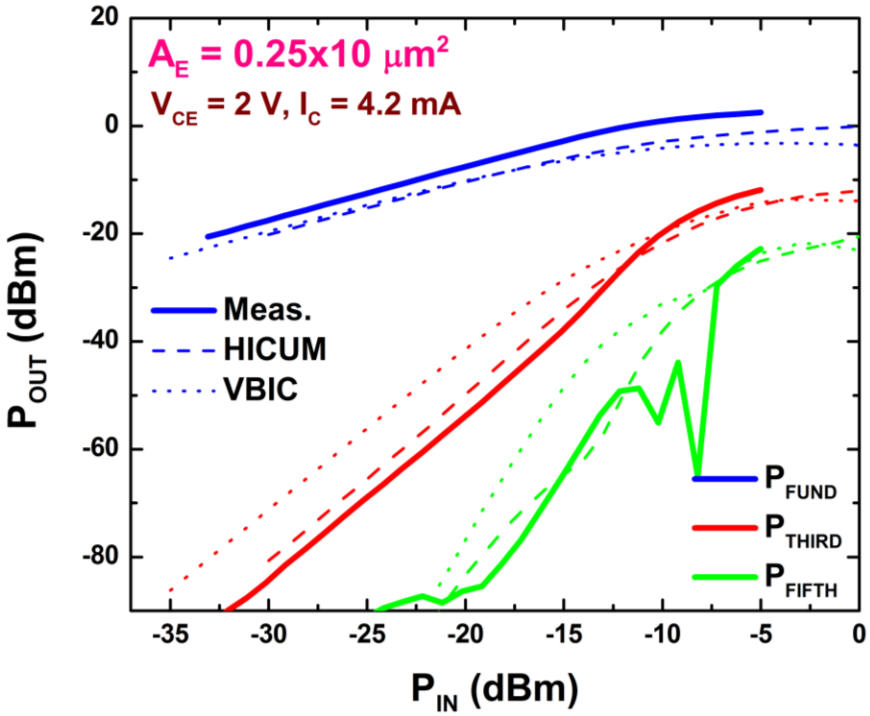

Figure 58: Comparison of measured and simulated fundamental (9 GHz), third-order (8.999 GHz) and fifth-order (8.998 GHz) tones for pnp SiGe HBT.

In Figure 58, the *dc* operating point of the *pnp* SiGe HBT was fixed and the RF power of the two input tones was swept to observe large-signal distortion and gauge modeling accuracy in this regime. The VBIC model captures the measured fundamental tone, but clearly over-predicts the third- and fifth-order tone power levels, leaving much room for error in high frequency circuit design. The HICUM model not only predicts the fundamental and the third-order tones accurately, it also does a very good job of capturing the fifth-order tonal power. Thus, for this C-SiGe platform, HICUM is the preferred model for reproducibility of large- signal effects such as gain-compression and higher-order distortion characteristics.

3.4.4 Conclusions

In this section, compact modeling concerns for accurate prediction of dynamic

range in RF front-ends were discussed. After a systematic and rigorous analysis, it was found that the HICUM compact model captures higher-order RF parameters such as gain, IIP3, IMD3, and IMD5 much better than the VBIC model, across a very wide range of *dc* bias conditions (from weak-saturation to near-breakdown). Measurement-to-model overlays at low V_{CE} and high I_C show modeling discrepancies even for the HICUM compact model. In personal communication with the inventor of the HICUM model, Dr. Schroter, it was realized that these discrepancies can be easily addressed by using the fee-based HICUM "Level2" version of the compact model.

CHAPTER IV

HIGH-PERFORMANCE DESIGN: FROM DEVICE TO CIRCUIT

4.1 Power Constraints and Weak-Saturation

In advanced SiGe HBTs, a germanium profile working in tandem with increased base doping levels helps to improve dynamic switching and noise characteristics of the SiGe HBT [81]. This makes them attractive for use in high-frequency, high-performance, low-noise circuits such as low-noise amplifiers (LNA) [67, 82-84], power amplifiers (PA) [38, 85-88], and voltage-controlled oscillators (VCO) [89-93]. For severely power-constrained wireless systems such as airborne surveillance systems, biomedical electronics, wireless devices, and other battery-biased systems, the inherent aggressive performance of SiGe HBTs can be potentially traded off for lower operating bias-currents and hence lower power dissipation [12]. Such systems require novel electronic techniques to be devised to make every milli-watt of power consumed count, e.g. for applications that are battery driven, a key requirement for circuits would be to operate using reduced voltage rails. This way, the *dc* power consumption of the circuit can be minimized while not compromising on performance. In addition to this appealing performance-bias current (e.g., f_T / f_{max} vs. I_C) tradeoff, many emerging applications also conserve power by lowering the operating voltage. The CMOS community has already developed new circuit design approaches to deal with the constraint of lower operating voltages [94]. A novel way of using the HBT in low voltage circuits, going against conventional wisdom, is to reduce collector-to-emitter voltage (V_{CE}) and operating the transistor in weak-saturation. Reducing voltage rails V_{CE} is directly proportional to reducing overall power consumption, since it minimizes the V_{CE}*I_C product. One would intuitively assume that low voltage operation in SiGe HBTs is not a viable approach, since lowering the collector-to-emitter voltage (V_{CE}) forces the bipolar transistor into saturation (e.g., if V_{BE} = 0.8 V, and V_{CE} = 0.3 V, the collector-base junction is forward-biased by 0.5 V).

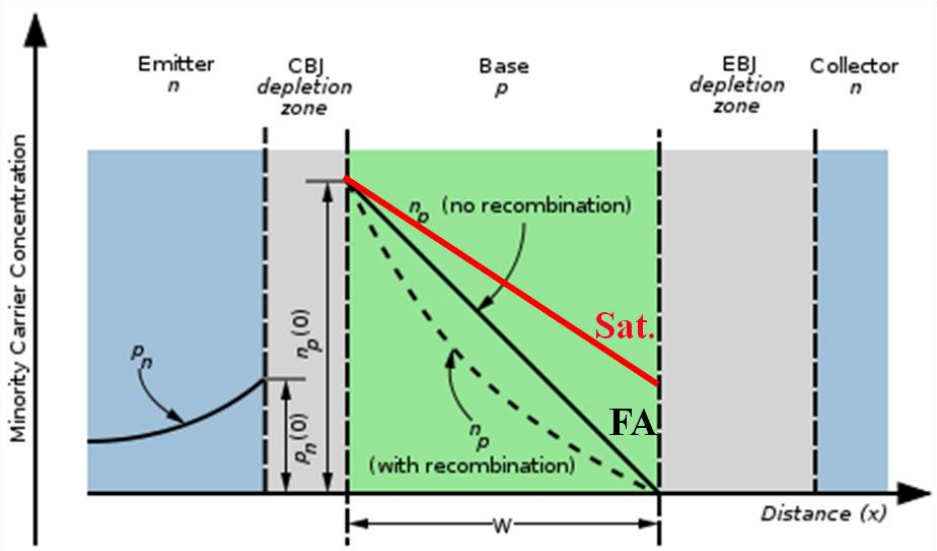

Figure 59: Minority charge carrier storage in the base of a Si BJT, under both forward-active and saturation modes of operation.

As shows in figure 59, in forward-active (FA) mode of operation in a Si BJT, the minority carrier density in the base is the area under the right-angled triangle with the solid black line as hypotenuse. When the transistor is operating in saturation regime (depicted by "Sat" in figure), the minority charge carrier density increases. In the saturation regime, the minority carrier density is the area under the polygon with the solid red line as the hypotenuse. Because of these additional carriers, it takes longer to completely deplete the base of all carriers when the transistor is switching off, making the transistor slower in its operation [58]. Thus, saturating a bipolar transistor floods the base region with excess minority carrier charge, severely degrading both *dc* and *ac* performance. Therefore, biasing the Si BJT in its saturation region was widely considered a very bad idea. In fact, bipolar circuit families such as CML/ECL were invented to *prevent* saturation in high-speed logic circuits The question answered in this work is: for power-constrained, low-frequency (e.g., < 5 GHz) circuits, is it possible to use the SiGe HBT in weak-saturation without overly compromising its RF performance metrics. It is known that SiGe HBTs enjoy RF-relevant advantages over CMOS at fixed scaling node (noise figure, 1/f noise, output conductance, g_m per unit area, matching, etc.); a SiGe

HBT operating in weak saturation might offer performance advantages over CMOS solutions at fixed (and highly constrained) power levels. Because of aggressive scaling, the base-widths of SiGe HBTs in advanced lithography nodes are very narrow. This, in addition to a selectively implanted collector (SIC) and a 25% germanium profile, translates into very high transconductance and very small transit times. The question is – in a third-generation SiGe platform, what happens to metrics such as transconductance, transit times, and current drive under weak-saturation operation? This chapter addresses this question for the first time by measuring the *dc*, *ac*, noise and linearity characteristics of weakly-saturated SiGe HBTs. The SiGe HBTs used in this study are from a commercially-available, third-generation, 130 nm SiGe BiCMOS platform [15], and were 0.12x6.0 μm^2 in geometry. The results from this chapter were published in [4] and [5].

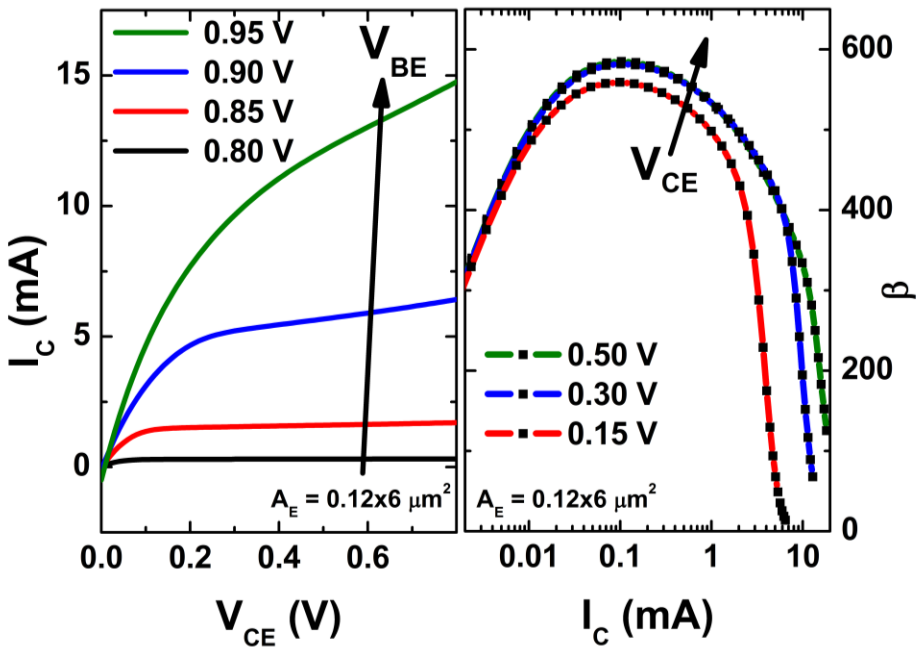

Figure 60: Left: Measured forced-V_{BE} output characteristics of a 0.12 x 6.0 μm^2 SiGe HBT. Right: Measured current gain (β) vs. I_C of a 0.12x6.0 μm^2 SiGe HBT for three different V_{CE}s.

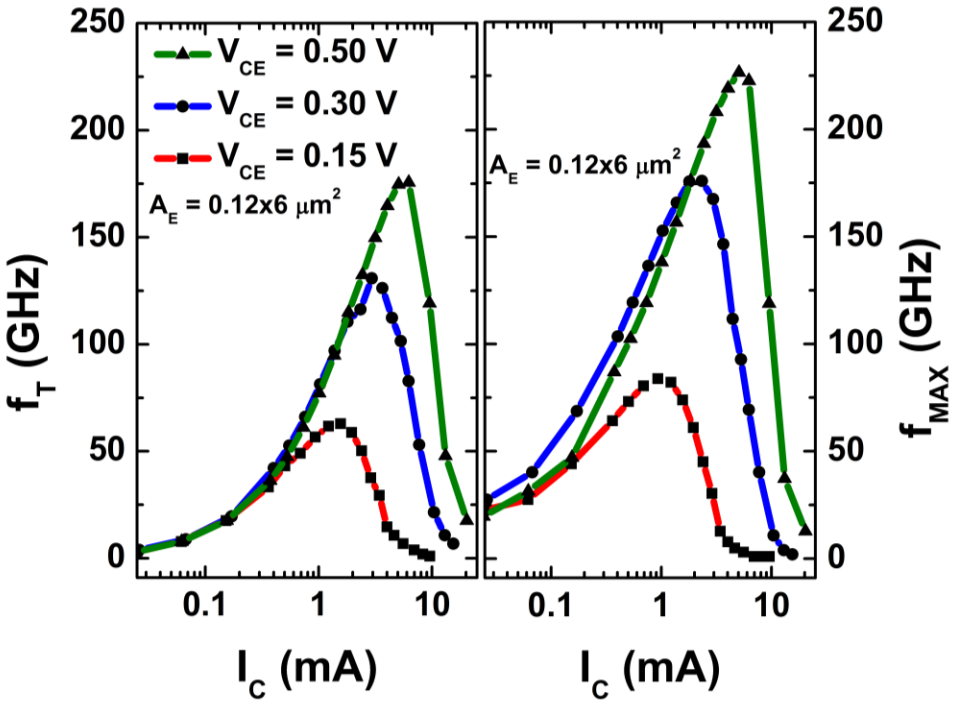

Figure 61: Measured f_T and f_{MAX} characteristics vs. I_C of a 0.12 x 6 μm^2 SiGe HBT taken at three different V_{CE}s.

4.2 Device: Measurement Results

I. DC Measurements

Figure 60 shows the output characteristics and the current gain (β) vs. bias current of the SiGe HBT in weak saturation. With both the E-B and the C-B junctions forward-biased, a collector current greater than 10 mA is still achieved, more than sufficient to bias the HBT at peak f_T, while the peak β remains above 400 in weak saturation. The current gain rolls off at high injection when in saturation, as expected (Figure 60).

II. AC Measurements

On-wafer high frequency measurements were performed, and pad parasitics were de-embedded at every frequency using the traditional open-short method [95]. As can be seen in Figure 61, the peak f_T and f_{MAX} of the SiGe HBT were found to be above 125 GHz at V_{CE} = 0.30 V and above 50 GHz at 0.15 V, more than acceptable performance for

low-frequency RF design. To obtain f_T / f_{MAX}, measured S-parameters were converted to H-parameters/Mason Unilateral Gain (MUG), both of which showed classical 20 dB/decade roll-off with frequency into saturation.

III. Noise and Linearity Measurements

III.A. Power Gain and Linearity (IIP3)

Power gain and small-signal linearity (IIP3) measurements were also performed on the SiGe HBT operating in a common-emitter configuration and terminated with 50 Ω load and source impedances. For linearity, the RF power was swept for two input tones (3.000 GHz and 3.008 GHz) ensuring a small-signal operation, and the output fundamental, third-, and fifth-order intermodulation (IMD) terms were measured. The third-order and first-order IMD data obeyed an ideal 3:1 slope, allowing extraction of the input third-order intercept point (IIP3) [12].

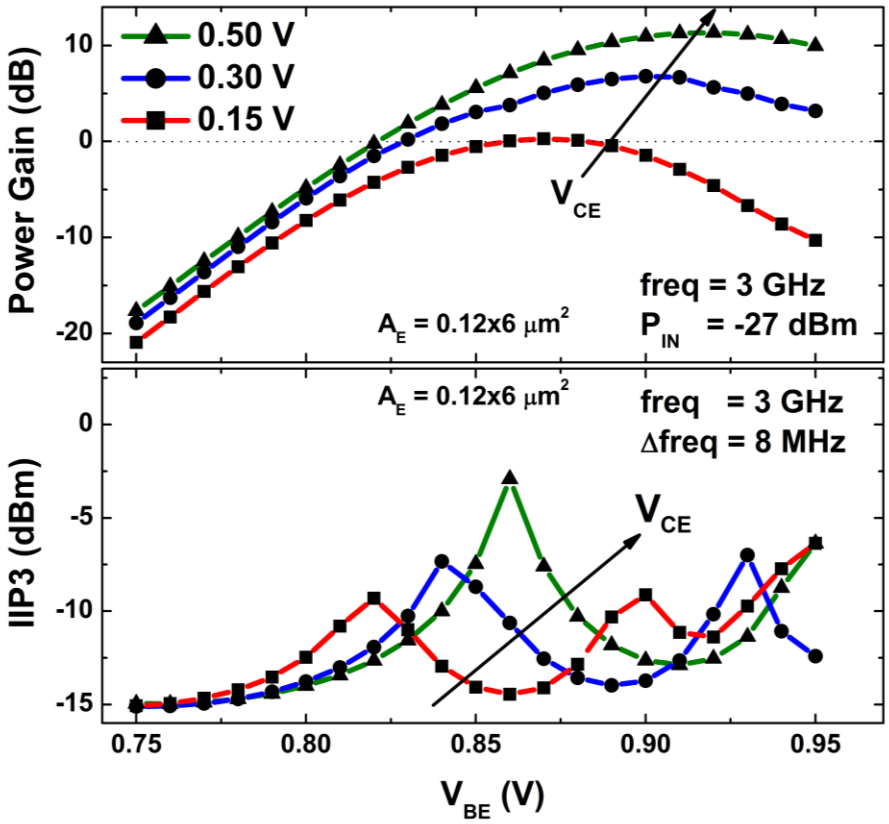

Figure 62: Top: Measured power gain versus V_{BE} for a 0.12x6 μm^2 SiGe HBT for 3 GHz input tone. Bottom: Two-Tone response of a 0.12 x 6 μm^2 SiGe HBT at 3 GHz input tone with 8 MHz offset.

Figure 62 shows measured IIP3 results, which reaches a peak above -8 dBm and -10 dBm at a V_{CE} of 0.30 V and 0.15 V, respectively. With increasing V_{CE} the peak IIP3 increases, consistent with the results reported in [28]. The "sweet-spot" for high linearity in the IIP3 curves can be exploited by designers to ensure high receiver sensitivity while still biased at low supply voltages. Other classical design approaches, feedback, degeneration, and load/source impedance matching, can also be used to further improve the linearity, as needed.

Figure 62 also shows RF power gain at 3 GHz. A power gain above 7 dB at V_{CE} = 0.30 V is achieved in weak saturation, while at 0.15 V the power gain is effectively zero,

rendering the device useless. As with linearity, power gain can be further enhanced using classical approaches, such as cascading, cascoding, and source/load impedance matching.

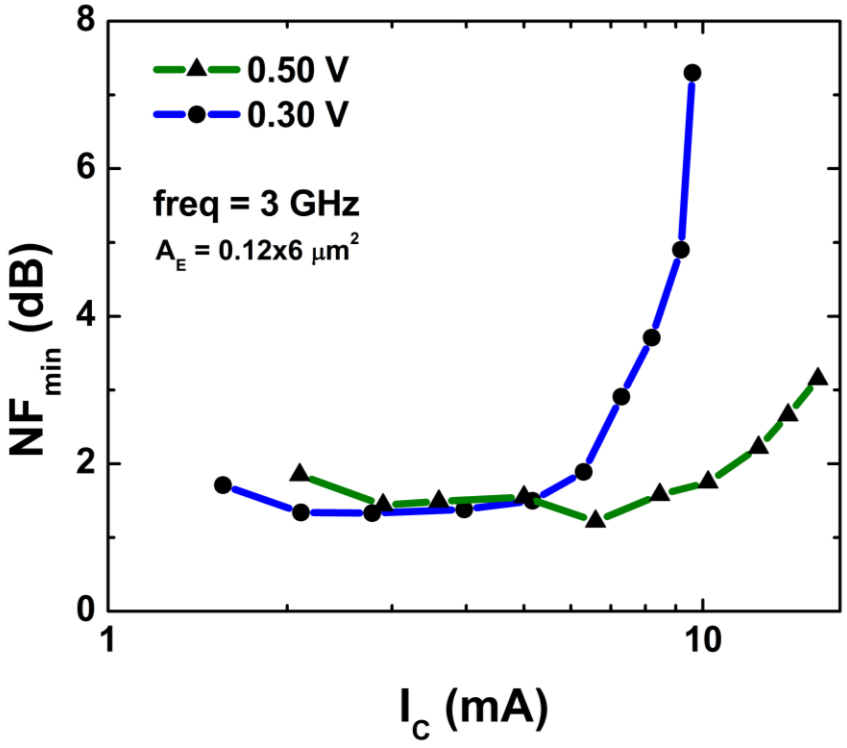

Figure 63: Measured minimum noise figure (NFmin) across bias for 0.12x6 μm^2 SiGe HBT at different V_{CE}s.

III.B. Noise Figure

Noise performance is clearly a key parameter for most RF applications, and here the noise was characterized in a load-pull setup, with the source impedance varied to find the optimum source impedance $Z_{s,opt}$ for minimum noise figure (NF_{min}) across bias at 3 GHz. Figure 63 shows the minimum noise figure (NF_{min}) across bias for different V_{CE}s. Sub-2 dB NF_{min} can easily be achieved in the weak saturation region. The impedance where noise figure is minimum ($Z_{s,opt}$) lies usually in the region of 150 Ω to 200 Ω, thus making impedance matching using lumped L-C components very easy in a RF circuit. It

is also seen in Figure 63 that NFmin is sub-2 dB across a wide bias range, allowing DC biasing of HBTs for simultaneous low noise & high gain performance.

4.3 Device: Takeaways and Summary

These results strongly suggest that SiGe HBTs operated in weak saturation represent a potentially viable bias regime for certain power-constrained circuits, especially for those that are intended for small-signal operation at very low voltages (e.g., LNAs). Respectable SiGe HBT RF performance metrics are clearly achieved at operating voltages above 0.30 V.

Table 2: Performance metrics of HBT and nFETs (same size & same power density as HBT). All RF and noise parameters are measured at 3 GHz.

	HBT (0.12x6 μm^2)		nFET (0.12x10 μm^2)		nFET (0.12x1x32 μm^2)	
	V_{CE} = 0.5 V	**V_{CE} = 0.3 V**	**V_{DS} = 0.5 V**	**V_{DS} = 0.3 V**	**V_{DS} = 0.5 V**	**V_{DS} = 0.3 V**
Peak f_T (GHz)	175	130	59	48	66	39
Peak f_{max} (GHz)	227	177	80	68	105	41
Peak power gain (dB)	11	6	-6	-8	4	1
Peak IIP3 (dBm)	-3	-8	7	5	5	4
NF_{min} (dB)	1.22	1.33	2.29	2.39	1.36	1.5

For an instructive comparison, we measured the RF performance of 130 nm nFETs, both of almost identical size (W/L = 10.0µm/130nm), and identical current drive capability (W/L = 32.0µm/130nm) to the SiGe HBT used in this study. The results of this comparison are summarized in Table 2. It is clearly seen that in all metrics of comparison (except IIP3), the HBT emerges as the winner. The FETs are less nonlinear than HBTs (hence higher IIP3) due to their square I-V relationship, as compared to an exponential I-V relationship in HBTs, which mathematically is the most non-linear relationship. However, the excellent power gain, noise figure, and ease of input impedance matching

of SiGe HBTs more than make up for their reduced IIP3. While clearly further "games" can be played in RF optimization of nFETs, these differences in "intrinsic" RF performance between the SiGe HBT and nFET are instructive.

4.4 Circuit: Motivation and Design Technique

The amplifier presented in this section builds upon the ability to utilize SiGe HBTs operating in the saturation regime for voltage/power constrained RF applications. Using this intentional saturation principle, an X-band SiGe LNA was designed that delivers high gain under very low voltage/power conditions, and which achieves record performance at reduced temperatures [5].

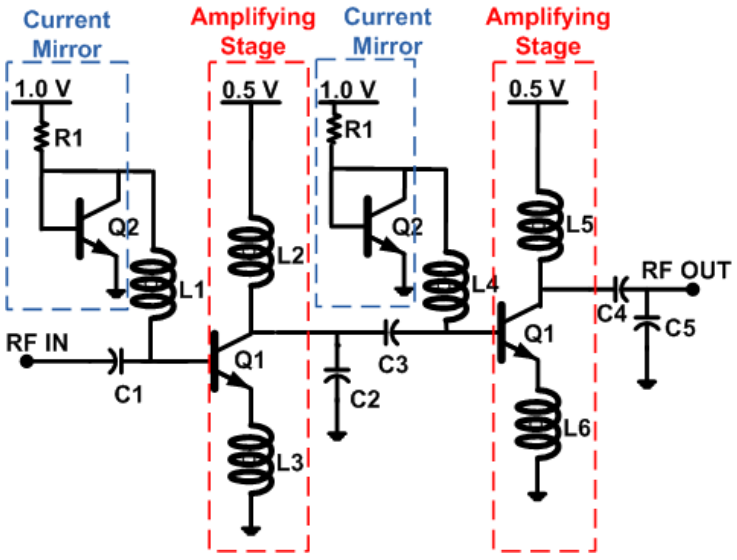

Figure 64: Schematic of the ultra-low voltage SiGe LNA.

The LNA was implemented in a commercially-available 0.13 µm SiGe technology and uses two cascaded common-emitter stages. Figure 64 shows the schematic of the LNA, and the values for the various components used in the amplifier design can be obtained from [5]. Using on-chip MIM capacitors and spiral inductors, the input L-C network (C1, L1, L3) serves the dual purpose of matching the input impedance of the SiGe HBT Q1 to 50 Ω to simultaneously provide low noise figure (NF) and excellent input reflection coefficient (S11), using a design approach described in [96].

Inter-stage matching (L2, C2, C3, L4) ensures good forward gain (S21), while matching at the output (L5, C4, C5) ensures excellent output reflection coefficient (S22) and circuit stability (K factor >> 1). Since the goal was to minimize power, the amplifier rail voltage V_{CE} of both amplifying stages is fixed at 0.5 V (the bias rail = 1.0 V). This greatly minimizes *dc* power consumption of the LNA (by minimizing the I_{CE}*V_{CE} for the common emitter stages) and makes the circuit suitable for voltage constrained applications. At the same time, since power budget was pre-decided in this case (2 mW), it did not leave the designer with much room to manipulate the *dc* currents, as is usually the procedure. Current mirroring (using Q1 and Q2) is used to self-bias the circuit and to ensure consistency in LNA performance as the temperature varies.

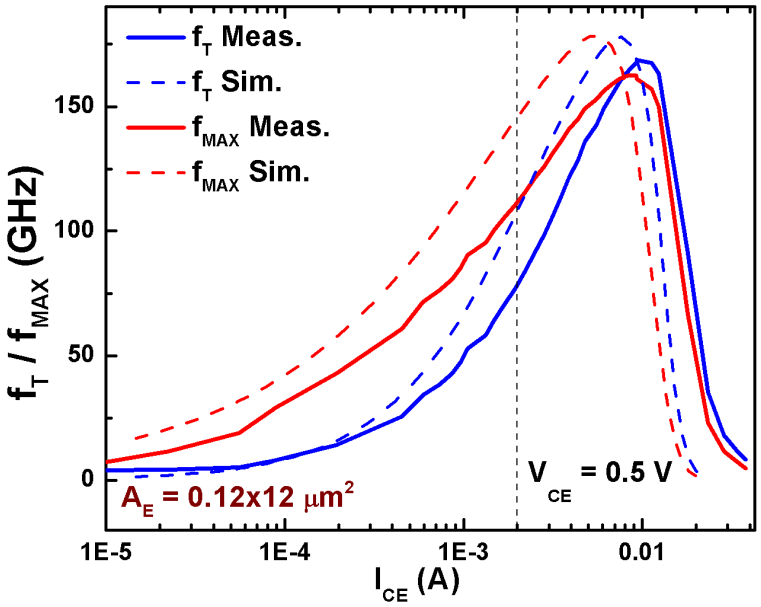

Figure 65: A comparison of simulated and measured f_T and f_{MAX} for a 0.12x12 μm^2 SiGe HBT biased in saturation (V_{CE} = 0.5 V).

Compact model inaccuracies (conventionally calibrated for only forward-active operation) pose the biggest challenge in designing circuits in the saturation regime, and can produce discrepancies between measured data and simulated results. RF measurements were performed on SiGe HBTs with a similar geometry as Q1, as shown in Figure 64.

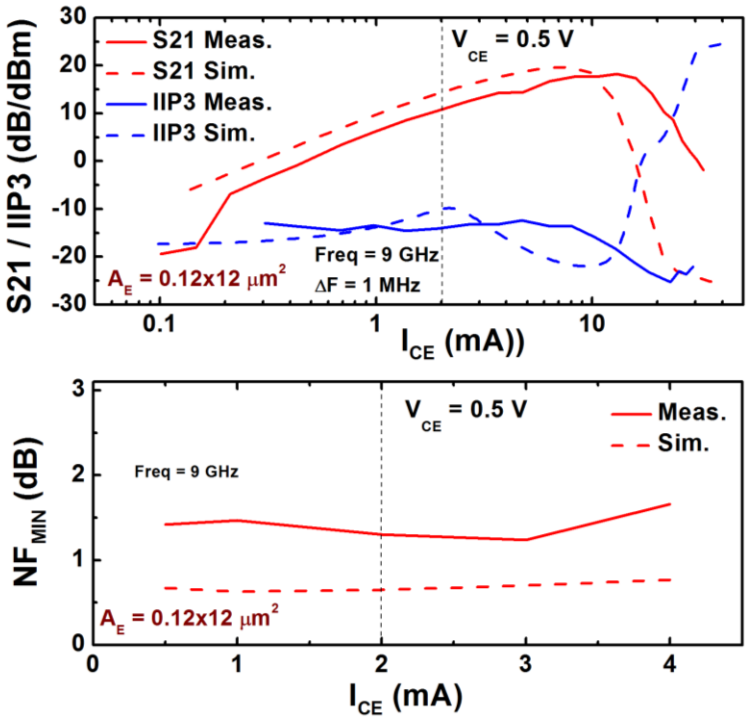

Figure 66: A comparison of simulated and measured power gain, IIP3 and noise figure for a 0.12x12 μm^2 SiGe HBT biased in saturation (V_{CE} = 0.5 V).

Figure 65 shows a comparison of measurement and simulation in weak-saturation for both f_T and f_{MAX} and Figure 66 shows a comparison of gain, IIP3 and NF of the SiGe HBT biased in weak-saturation. The vertical dotted line shows the *dc* bias current for the amplifying HBT Q1 in the LNA. While impressive performance metrics can be achieved by SiGe HBTs biased in saturation, it becomes very clear that commercial compact models do not accurately capture these performance metrics well. However, these modeling deficiencies should be easily correctable.

4.5 Circuit: Measured Results

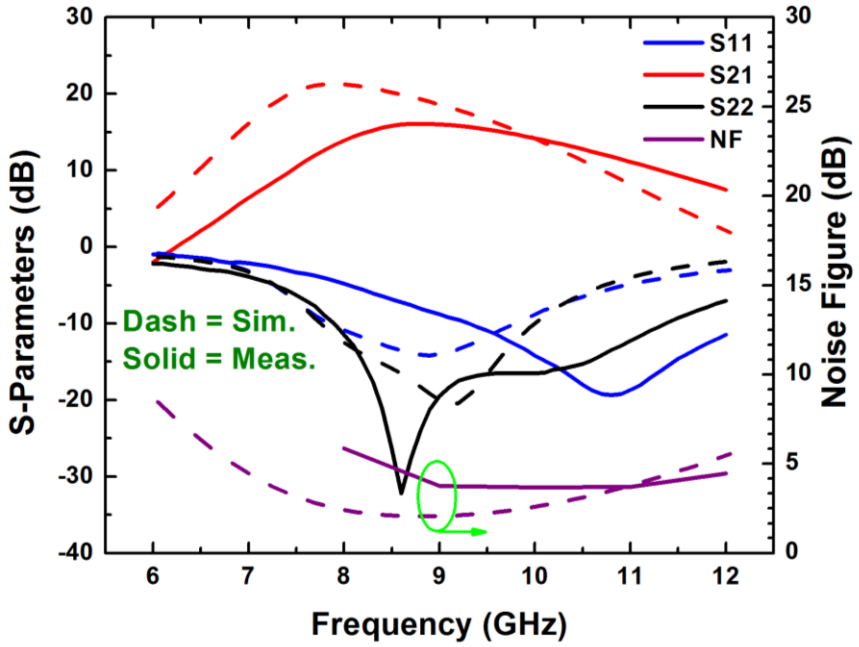

Figure 67: Comparison of measured and simulated S-parameters and noise figure of the saturated LNA.

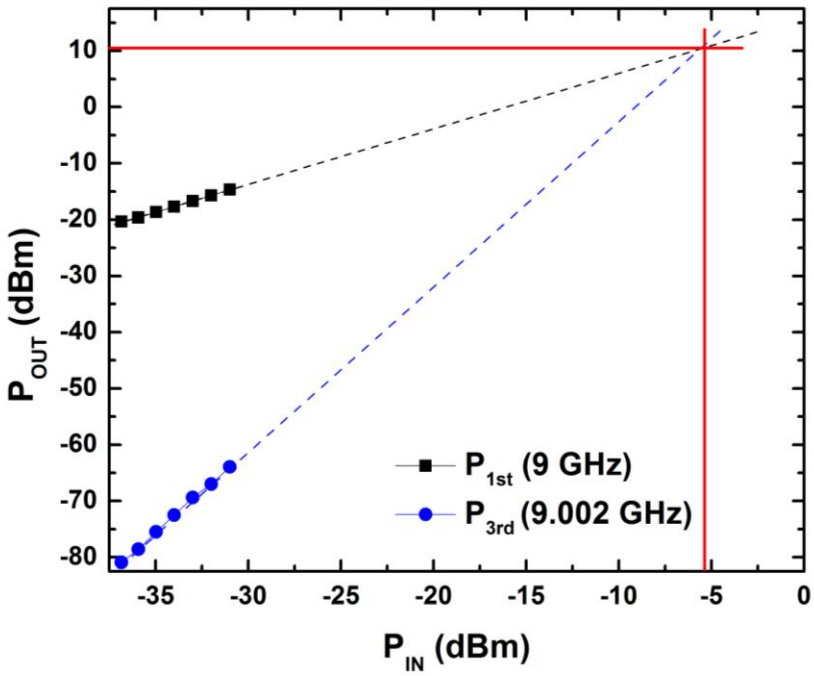

Figure 68: Measured 2-tone response of the LNA.

Figure 67 shows the measured and simulated S-parameters and broadband noise results of the saturated SiGe LNA. The simulated results were parasitic extracted from the actual layout, and suggest that a gain of 22 dB and a sub-2 dB NF should be achievable in principle. On-wafer measurements using a 1.0 V *dc* supply yield an LNA gain (S21) of 16.7 dB at 9 GHz while only consuming 2.4 mW dc power (0.5 V*2.05 mA + 1 V*0.19 mA per stage, as measured on die). The input and output reflection coefficients are less than -10 dB at 9 GHz. The noise figure was measured to be 3.5 dB. As in Figure 68, the OIP3 and IIP3 of the LNA were measured to be 10 and -6 dBm, respectively. The P1dB of the LNA (not shown), was -5 dBm. A photomicrograph of the LNA is shown in Figure 69. Including the GSG pads, the die area is 900 x 830 μm^2.

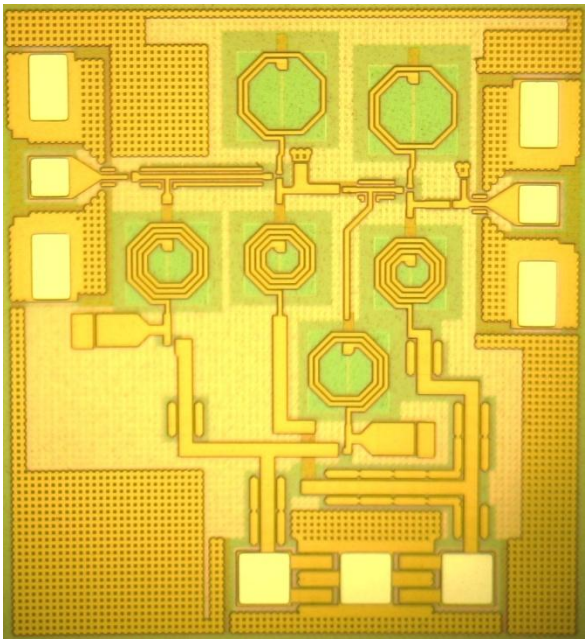

Figure 69: Photomicrograph of the saturated LNA. It measures 900x830 μm^2 including GSG pads.

4.6 Circuit: Over-Temperature Performance

It was shown in [67] that a voltage-biased cascode SiGe HBT LNA designed for room temperature exhibits an increase in small-signal gain S21 as the temperature decreases. Keeping the LNA performance stable across temperature requires manipulating the *dc* bias of the circuit as a function of temperature, thus making it

difficult to integrate into a system. Because our intent here was to also demonstrate the usefulness of saturated LNA's for cryogenic operation, this LNA was designed to be self-biased from a fixed voltage source (1 V in this case), for all temperatures. To help ensure that the LNA performance remained robust as the temperature was varied, the following techniques were also employed:

1. We traded off the natural increase in transistor peak f_T/f_{MAX} with cooling (at fixed I_C) for a lower I_C at fixed performance (f_T).
2. We employed a current-mirror based current source (transistor Q1/Q2 and resistor R1) to bias the base of the amplifying HBT Q2 in both stages.

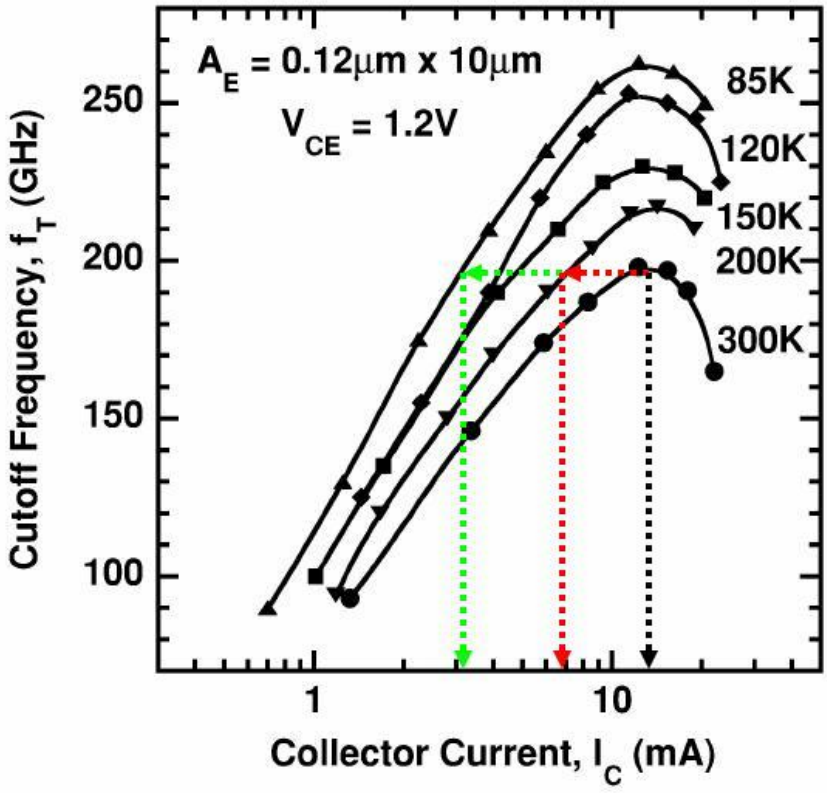

Figure 70: f_T increases with decreasing temperature, enabling the HBT to be biased at much smaller collector currents at 200 K and 85 K to achieve similar ac performance as 300 K.

It has been shown in [11] and [97] that the peak f_T and f_{MAX} of SiGe HBTs increase with cooling. As temperature decreases from 300 K to 85 K, the peak f_T in this technology platform increases by 60 GHz. Thus, at low temperatures, the SiGe HBTs can

be biased at much smaller collector currents to achieve the same f_T and f_{MAX} (hence small-signal gain, S21) as at 300 K. An example of this design approach is shown in Figure 70, reproduced from [97]. The peak f_T of the SiGe HBT at 300 K is about 200 GHz, and is attained by biasing the HBT at a collector current of 13 mA. A similar f_T can be achieved, however, at 200 K by biasing the HBT at only 7 mA (as shown by the red line), and at 85 K by biasing the HBT at only 3 mA (as show by the green line)! This approach of dramatically reducing the bias current while maintaining fixed *ac* performance approach is instrumental in reducing *dc* power consumption at low temperatures for this saturated LNA, producing truly impressive power numbers for a given level of performance.

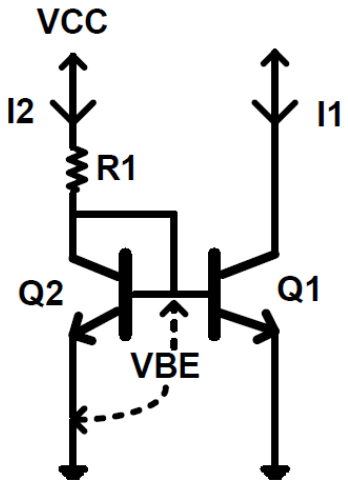

Figure 71: Current-source employed in the saturated LNA. Q1 doubles as the amplifying stage.

The current-mirror based current source, shown in figure 71, ensures a self-biased LNA. A simple *dc* load line analysis of transistor Q2 shows that it is constrained by the following equations:

$$I_2 = \frac{V_{CC} - V_{BE}}{R_1} \tag{17}$$

$$I_2 = I_S * exp\left(\frac{V_{BE}}{KT/q}\right). \tag{18}$$

When V_{CC} is applied to the circuit in the off-state, the V_{CE} of Q2, and hence V_{BE}, is pulled up to rail V_{CC}, and a large current starts to flow through Q2, determined by equation 17. This current passes through R1 and ensures a voltage drop across it, thus reducing the V_{CE}/V_{BE} of Q2. Gradually, a quiescent *dc* bias point is established, V_{BE} is now fixed, and a corresponding I_1 starts to flow through the amplifying stage.

With decreasing temperature, the V_{BE} of the HBT naturally increases [97]. According to equation 18, as the temperature drops a reduced current I_2 flows through Q2 and thus a reduced current is mirrored through amplifying stage Q1. By careful selection of the transistor geometries and resistance R1, the amplifying stage at low temperatures can be made to operate at similar *ac* performance as at 300 K, while drawing only a small fraction of the current. Thus, using a current-mirror based biasing scheme, a self-biased low power/voltage LNA with very attractive cryogenic performance can be obtained.

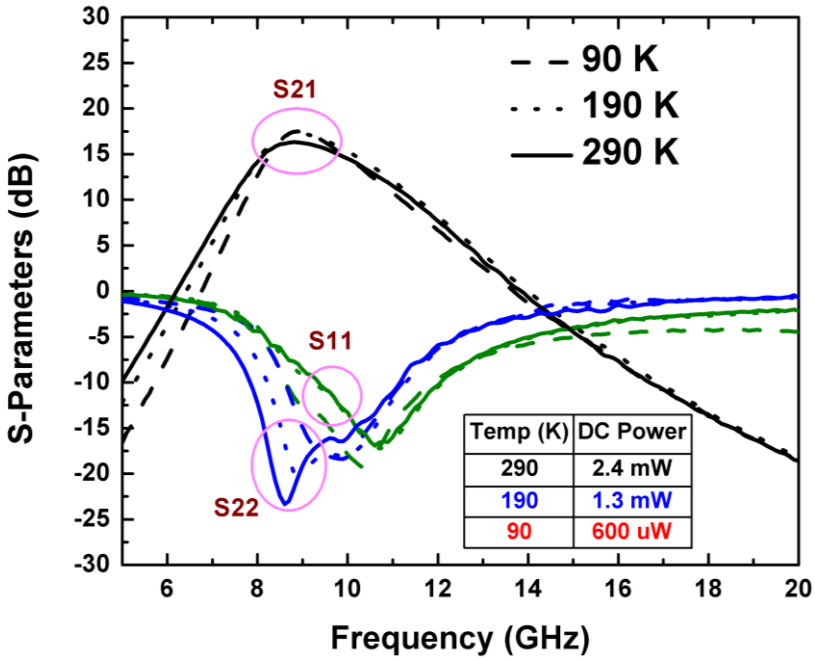

Figure 72: Measured S21 (black), S11 (green), and S22 (blue) of the saturated LNA at 3 different temperatures (90K, 190K, and 290K). Inset shows dc power consumption as temperature varies.

Figure 72 shows that the S-parameters of the weakly saturated LNA are consistent over a 200 K wide range of temperatures, unlike that found in [67]. The inset shows the

dc power consumption of this saturated LNA at three temperatures. The saturated LNA achieves a gain of 17.5 dB at 90 K, while consuming only 600 µW of *dc* power! To our knowledge, these are record numbers for a SiGe HBT X-band LNA operating at cryogenic temperatures.

4.7 Circuit: Benchmarking

Table 3: Comparison with other SiGe LNAs

Reference	Frequency (GHz)	Gain (dB)	P_{DC} (mW)	NF (dB)	OIP3 (dBm)	FOM1	FOM2	Supply Voltage
This work	9	16.7	2.4	3.5	10.7	6.95	1.39	1.0 V
[98]	10	10	2	1.98	10	5	2.52	1.5 V
[99]	9.5	11	2.5	2.78	1.9	4.4	0.22	2.5 V
[100]	10	19.5	15	1.36	20.3	1.3	5.25	2.5 V
[101]	10	17	2.7	2.7	4	6.29	0.34	1.5 V
[102]	8.2	22	4.4	1.6	--	1.53	--	1.8 V

$$FOM1 = \frac{Gain(db)}{P_{DC}(mW)} \tag{19}$$

$$FOM2 = \frac{OIP3(mW)}{P_{DC}(mW) * NF(dB)} \tag{20}$$

A comparison with other X-band 300 K SiGe LNAs is shown in Table 3. Figure-of-merit #1 (FOM1) (equation 19) captures a key RF front-end requirement; namely the LNA's ability to amplify incoming RF signals for a given level of expended *dc* power consumption (clearly, the larger the FOM the better). The saturated low voltage/power SiGe LNA exhibits highest FOM1, while operating off the lowest *dc* supply voltage! For FOM2 (equation 20), which also includes noise and linearity (again, the larger the FoM the better), the saturated LNA, while not the best, is still competitive, and further improvement in noise figure is envisioned with more refined saturation models. Noise-Figure and IIP3 of the LNA under cryogenic temperatures was not measured, but it can be confidently estimated from data presented in [103] (Fig. 74, Fig. 82) that those metrics

will definitely improve.

4.8 Summary

In this chapter, a novel and unconventional mode of transistor operation – the weak-saturation regime – is discussed in detail. Measurements (*dc*, *ac*, and RF parameters) at the transistor level show that in aggressively scaled third-generation SiGe HBTs, the device does not exhibit major performance degradation when biased in weak-saturation regime. A low-voltage, low-power SiGe X-Band LNA based on the same principle is designed. The LNA provides the maximum RF gain per *dc* power compared to all other SiGe LNAs, making it a front-running contender for extreme environment applications, which necessitate low-voltage and power constrained circuit design. In addition to its extremely low power consumption, the LNA is designed to be temperature invariant. At 90 K, for instance, the LNA provides 17.5 dB RF gain at X-Band while consuming only 600 μW *dc* power. This is a record performance to the best of the authors' knowledge, and can be very useful for systems operating at cryogenic temperatures.

There are some implications that need to be acknowledged before operating the HBT in weak-saturation. Firstly, only third-generation (and beyond) SiGe HBTs will yield useful performance when operated in weak-saturation. Because they have the most "performance-to-burn", it can be traded off for low power operation at smaller frequencies (<10 GHz). This, however, isn't a show-stopper as SiGe BiCMOS technology advances to 500 GHz performances at room temperature. Secondly, even with V_{CE} set to 0.5 V, we still need a minimum voltage of roughly 0.85 V to turn on the base-emitter junction. While a SiGe circuit working off a 0.85 V rail would still have the

lowest supply-voltage reported, methods needs to be devised (pFET current mirrors, for instance) to bias the base-emitter junction from an even smaller rail of 0.5 V. Lastly, the weak-saturation principle is not recommended for designing large-signal circuits such as power amplifiers, or high-drive oscillators. Due to reduced voltage rails, the *ac* signal at the output of the amplifying HBT will saturate due to gain-compression very easily. Thus, the weak-saturation approach is best suited to small-signal circuit design like LNAs, or variable gain amplifiers.

CHAPTER V

HIGH-PERFORMANCE QUADRATURE MODULATOR DESIGN

5.1 Introduction

SiGe HBTs have naturally been a technology of choice for use in wireless applications. Low noise metrics (due to a heavily doped base) and very high transconductance (due to its bandgap-engineered nature) have made SiGe technologies a perfect fit for use in high-performance RF front-end design. These aggressive performance metrics allow SiGe HBTs to overcome the very minor disadvantage they possess over their FET counterparts in terms of small-signal RF linearity (intermodulation). It is a well-known fact that SiGe HBTs are more nonlinear than FETs, due to their exponential I-V current relationship [12], as compared to a square relationship in FETs. This implies, for identical tones incident to an HBT and an equivalent FET, the HBT will have more prominent intermodulation terms. This fact can be put to good use to design circuits that rely on the inherent nonlinearity of the active device, e.g. a mixer. Recently, there has been a slew of literature on high-performance mixer design using SiGe technologies, especially at the higher-end of the frequency spectrum [104, 83, 13, 105].

In this chapter, the design of an upconverting In-phase/Quadrature (IQ) modulator for use in a base-station is described. An upconverting modulator converts the information-bearing baseband (BB) signal to an RF signal for wireless propagation by mixing it with a spectrally-clean high-frequency local-oscillator (LO) signal. Such circuits can be used as direct-to-RF modulator in digital communications systems such as GSM, CDMA, and WCDMA base-stations, and QPSK and QAM broadband wireless access transmitters. Using complex modulation schemes, such circuits can also be used as perfect Intermediate Frequency (IF) modulators in Local Multipoint Distribution Systems (LMDS). The modulator in this chapter is implemented as a double-balanced mixer,

meaning that it suppresses both input signals (BB and LO tones), and only mixed tones are generated at the output [96]. The advantage of employing a double-balanced topology is that it lends itself to higher linearity and displays better frequency isolation between all ports compared to single balanced mixer. The biggest disadvantage of using a double-balanced topology is that higher LO drive levels are required to commutate the LO-path transistors. This, unlike battery-driven wireless applications, is not a major issue for base-station applications, where strong LO signals can easily be generated on-chip at the expense of greater *dc* power consumption.

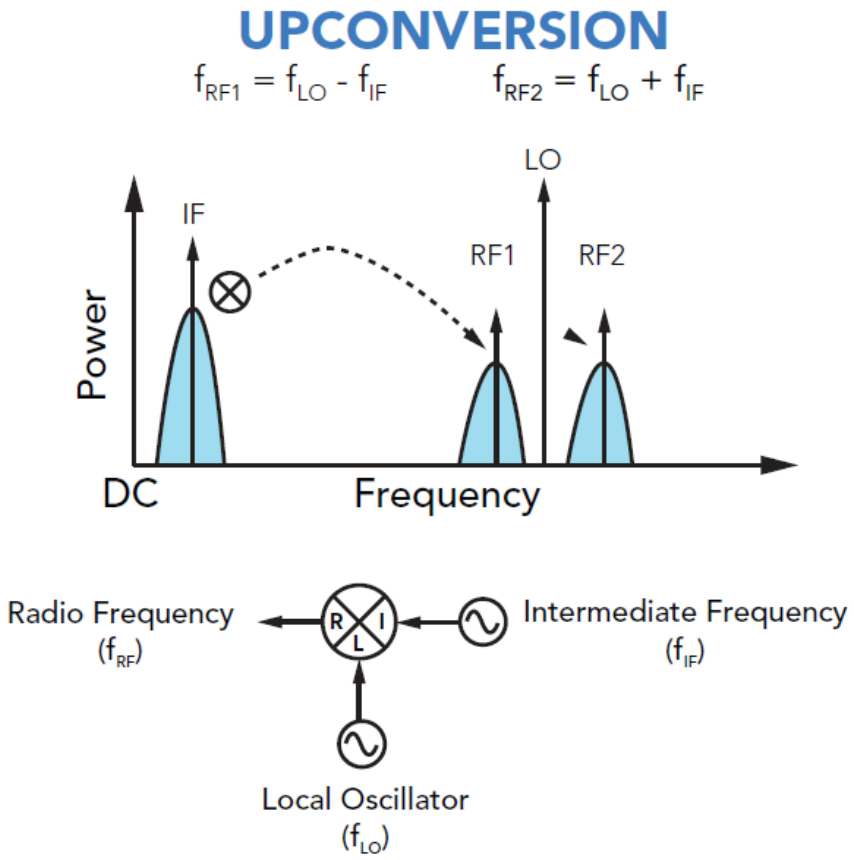

Figure 73: A simplified pictorial representation of upconversion in RF mixers.

Figure 73 shows the mechanism of upconversion in a double side band mixer. The information-bearing signal is present very close to DC, at IF or baseband frequencies, with sub-gigahertz frequencies. When mixed with an LO signal, two intermodulation

products are generated at RF1 and RF2. The mixing products can be determined by the following equation:

$$f_{RF} = n * f_{LO} \pm m * f_{IF}, \tag{21}$$

where m and n are integers. In addition to the signal of interest (when m = n = 1), various harmonic terms are created as a by-product of mixing. Elimination of these frequencies is a key goal in mixer design, and directly corresponds to improving the linearity of a mixer. For the case when two tones IF_1 and IF_2 are incident at the mixer IF port, the mixing products generated are:

$$f_{RF} = \pm m_1 * IF_1 \pm m_2 * IF_2 \pm n * f_{LO}. \tag{22}$$

In equation 22, the desired output tones are generated for $m_1 = 0$, $m_2 = n = 1$, and $m_2 = 0$, $m_1 = n = 1$. The third-order mixing terms are generated for $m_1 = 1$ and $m_2 = 2$, or $m_1 = 2$ and $m_2 = 1$. They are called third-order terms because the sum of coefficients of IF_1 and IF_2 equals 3. As in the case of an amplifier, discussed in Section 1.3.2, the input power of the IF tones can be swept, and intercepts can be determined for the point where the extrapolated fundamental (desired) frequencies intersect with the extrapolated third-order mixing terms.

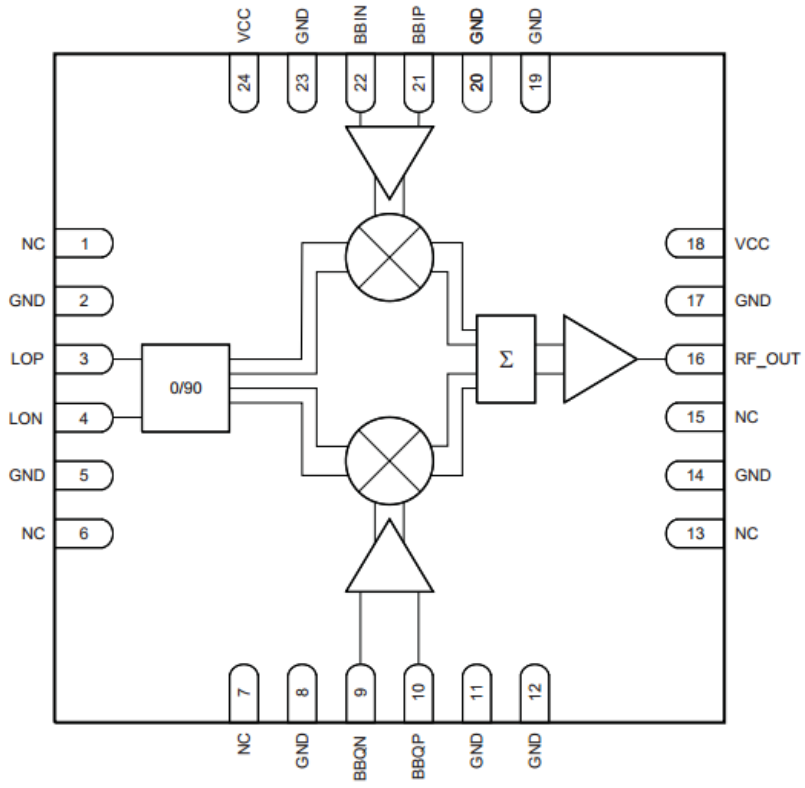

Figure 74: A functional block diagram of the upconverting modulator, taken from [106].

In this chapter, the design of an upconverting modulator (implemented as a double-balanced mixer) is described. Figure 74 shows the functional block diagram of the entire chip (TRF3705 by Texas Instruments), the older version of the current chip under production. This chapter focuses only on the design of the mixer circuit, and not on the associated digital control circuits, on-chip LO generation, polyphase filters, or the output amplifier. As a starting point, a systematic analysis of the device-level linearity was performed, and the device with best linearity performance was chosen for the circuit design. This step was important, since the PDK used for design did not support scalable HBT. Instead, the designer is given a few discrete HBT geometries to work with. The final IQ modulator has a bandwidth of 0.4 - 4GHz, simulated OIP3 greater than +30 dBm, simulated conversion gain greater than +17 dB, simulated compression point greater than 12 dBm, and a noise floor of -150 dBc/Hz.

5.2 Device: Linearity and Geometrical Scaling

Before commencing the design of the high-performance modulator, all the transistor geometries supported by the PDK were characterized to evaluate RF properties such as gain, IIP3, and OIP3. Measurements across the entire bias-spectrum (from weak-saturation to near-breakdown, with swept I_C) were performed with 50 Ω load and source terminations.

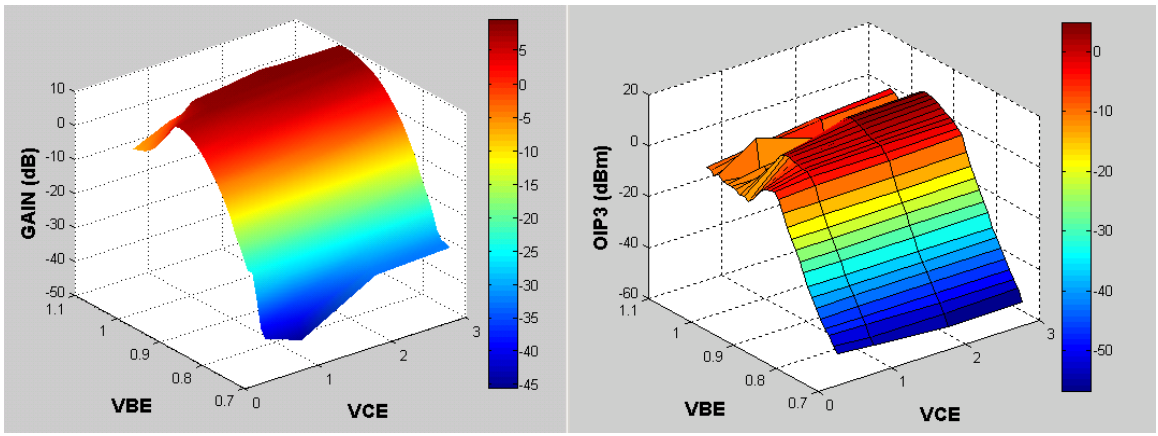

Figure 75: 3-D rendering of npn SiGe HBT (0.3x6.4 μm^2) gain and OIP3 at 2.5 GHz as a function of changing V_{BE} and V_{CE}. High values of gain and OIP3 are attainable even at smaller V_{CE}s, thus enabling low power high linearity design.

Figure 75 shows the measured gain and OIP3 results for a device of geometry 0.3x6.4 μm^2. Two tones of 2.5 GHz and 2.508 GHz were presented to the DUT input, each at a power of -30 dBm. It can be seen that even for very small values of V_{CE} (e.g. 0.5 V), the DUT can attain very high gain and OIP3 values. Measured OIP3 increases with increasing V_{CE}, as has been reported previously [1]. This multi-dimensional *dc*-bias characterization established the fact that these HBTs can perform at aggressive performance specifications across a very wide range of bias points.

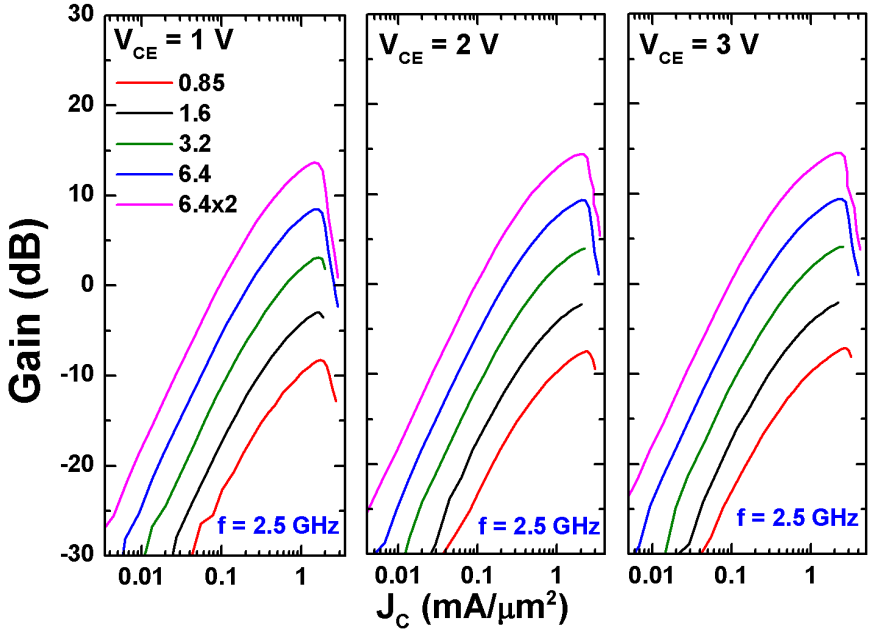

Figure 76: Power gain (in dB) as a function of collector current density for npn SiGe HBTs with varying emitter lengths and V_{CE}.

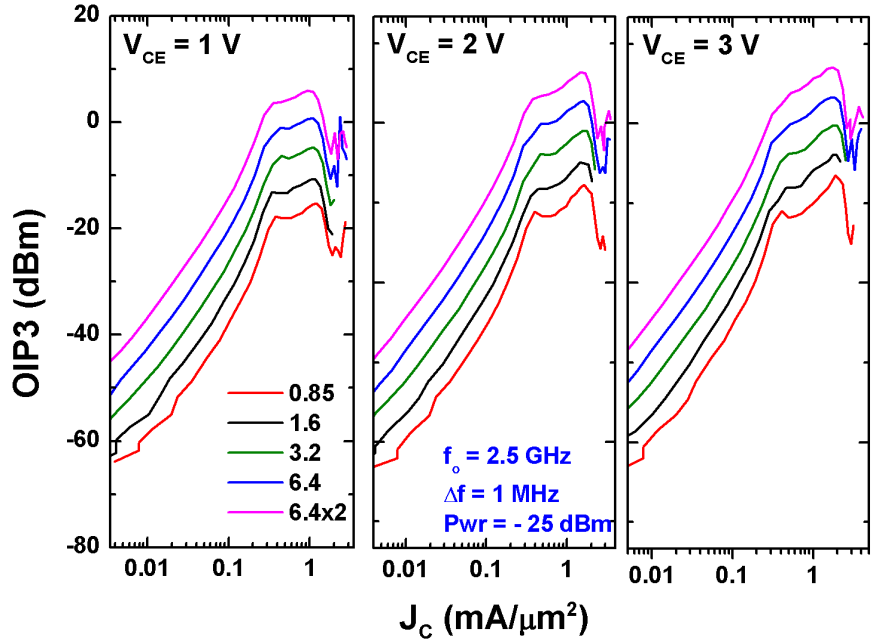

Figure 77: Output IP3 (in dBm) as a function of collector current density for npn SiGe HBTs with varying emitter lengths and V_{CE}.

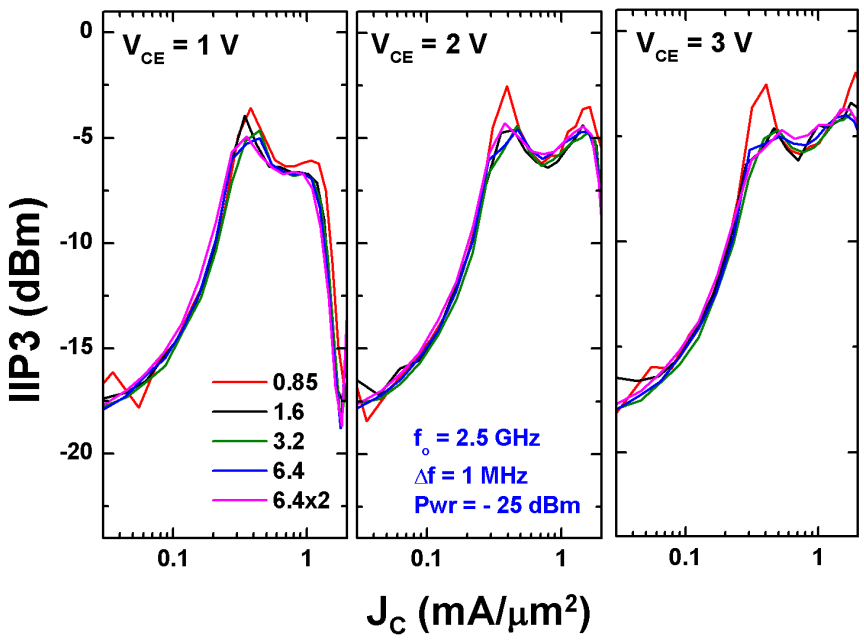

Figure 78: Input IP3 (in dBm) as a function of collector current density for npn SiGe HBTs with varying emitter lengths and V_{CE}.

Figures 76, 77, and 78 show the measured gain, OIP3, and IIP3 for all the *npn* SiGe HBTs in the PDK with increasing emitter lengths. The legend corresponds to discrete emitter-lengths of each HBT. In this process, the devices were not scalable, and the designers had to rely on "arraying" the devices with discrete geometries to realize larger HBT cores.

From Figure 76, it is seen that increasing the device geometry leads to increased RF gain. This finding can trace its origin back to the increasing transistor transconductance with increasing geometry. Increasing the emitter area in SiGe HBTs leads to increased *dc* collector-current draw, which in turn leads to increased transconductance. This, in turn, leads to increased gain in an HBT configured in a common-emitter configuration. When plotted over collector current density (J_C), we can see that the curves align perfectly on top of each other, their values scaling in the same ratios as their geometry does.

Figure 78 shows the IIP3 of all the *npn* SiGe HBTs in the PDK, plotted as a function of collector-current density (J_C). It can be seen that the curves overlap almost

perfectly. This result can be explained, in part, by the fact that at low J_C, the IIP3 is very dependent on g_m nonlinearities [12]. As the g_m scales, so would the IIP3. Thus, when normalized by emitter area, the curves happen to overlap almost perfectly. In other words, even though the values of measured RF gain increase with increasing geometry, their slope (rate-of-change) remains exactly similar. Because linearity depends critically on rate of change of I_C (hence g_m), or C_{BC} as a function of varying *dc*-voltage, the IIP3 remains the same across J_C even for increasing device geometries.

Combining the above two results, it is naturally seen that the OIP3 of all the measured HBTs scales with geometry. This implies that the larger the HBT size, the higher its measured OIP3 will be. This result is key to the modulator design, because it gives us a handle on which discrete HBT geometry to pick and array to realize a very high-linearity quadrature modulator. For our work, the geometry of 0.3x6.4x2 μm^2 was chosen as the "workhorse" device.

5.3 Circuit: Topology and Description

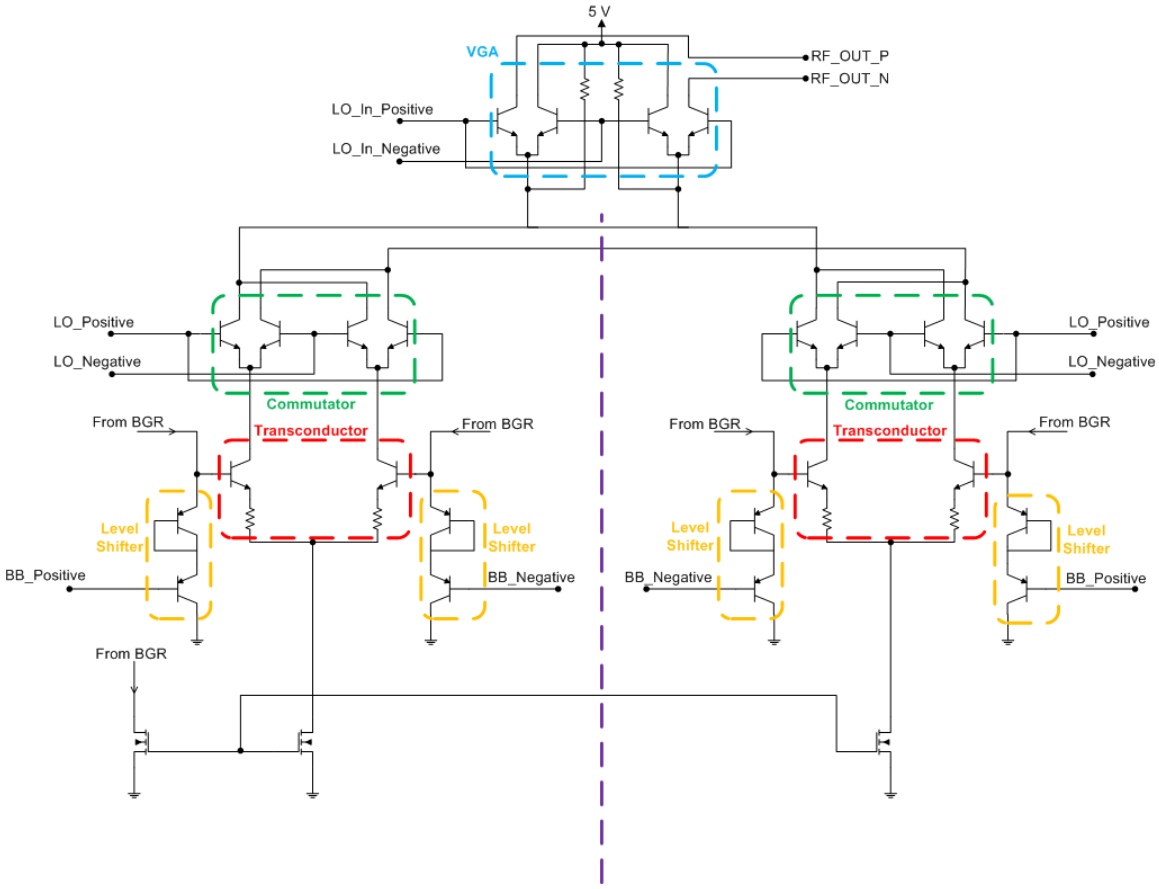

Figure 79: Simplified Schematic of the high-linearity quadrature modulator.

The topology chosen to implement the IQ quadrature modulator was a Gilbert cell block [107], followed by a variable gain amplifier, as shown in Figure 80. In-phase and quadrature signals worked to cancel out the unwanted mixed signal image at the output. The two balanced mixers within the image reject mixer are driven in quadrature by the BB signal. The LO drive to each mixer is in-phase and the RF output is combined in quadrature.

As established in the previous section, all transistors were arrays of the 0.3x6.4x2 μm^2 *npn* SiGe HBT. The purple shaded line divides the symmetric I- and the Q-paths of the signal. Using this topology, an output-referred third-order intercept point of +30 dBm

was obtained in simulation, as well as a conversion gain of >17 dB, across a 0.4 – 4 GHz frequency band.

1. Level Shifter

The *pnp* SiGe HBTs in the shaded yellow rectangle constitute the level-shifter stage of the design. The quadrature modulator chip is meant to interface with a Digital-to-Analog Converter (DAC) that generates the baseband signal. For this chip, the companion DAC is the "DAC3484" [108] by Texas Instruments, which is a very high dynamic range, low power, quad-channel, 16-bit DAC with a maximum sample rate of 1.25 GSPS. The voltage-swing of the output signal from every DAC is centered around a common-mode voltage. The lower bounds of the DAC output voltage-swing is usually the ground node. Therefore, a higher common-mode voltage translates into higher output signal-swing (~2*$V_{common\text{-}mode}$). In this way, a higher common-mode DAC voltage leads to highly linear output signal. The DAC3484 has dual common-mode output voltages, that of 0.25 V and 0.5 V.

To allow these outputs to be usable by the transconductor stage of the modulator, *dc* level-shifting must be employed [58]. Since an *upward* level-shift is desired (from 0.5 V common-mode DAC voltage to ~2*V_{BE} of the transconductor *npn*), *pnp* SiGe HBTs are employed in the common-collector configuration. Common-collector topology ensures voltage-buffering, which ensures that the baseband signal is kept in the voltage domain. In this circuit, the incoming baseband signal is increased by two V_{BE} voltages, once from the common-collector configured *pnp* SiGe HBT, and again from the diode connected *pnp* SiGe HBT. Ideally, Schottky diodes could have been employed for the same purpose. For this circuit however, their usage was ruled out because the reliability of such diodes over large signal-swings was not very well understood by the process design team. In addition, the built-in voltage of the diodes was found to be only ~0.5 V, thus requiring three diodes to achieve a level shift of around 1.5 V. This would have significantly increased layout complexity, due to requiring four instances of level-shifter

circuit in the modulator block. The biasing of the level-shifter stage is performed using a band-gap reference circuit, which was available on chip.

2. Transconductor

The transconductor block, depicted by the red rectangle in Figure 79, is the most crucial stage of the design – it is the stage where the incoming baseband signal is converted from the voltage-domain to the current-domain. At its core, the transconductor works in the same manner as a resistor – for a given applied baseband voltage across its terminals, it generates a proportional current output, thus acting as a V-to-I converter. The IQ modulator outputs, all the way up to the RF output, were kept in the current domain to minimize V-to-I conversions and resulting linearity issues. The topology employed for realizing the transconductor for the baseband signals is a simple differential pair with resistive degeneration, as in the classical Gilbert cell [107]. While the simplified schematic in Figure 79 shows only one pair of degeneration resistors, the actual modulator circuit has switchable degeneration resistors of three different values, to control the linearity and the gain of the transconductor. The various degeneration resistors can be switched in and out of the circuit using digital pass-gate switching. A higher value of degeneration resistors leads to increased linearity, but at the expense of lost RF conversion gain [58]. Thus, to tune linearity of the modulator, the biggest tuning knobs in the design were degeneration resistance, number of transistors in each diff-pair, as well as collector current. To reduce the noise floor, having a very small input resistance by arraying the diff-pair HBTs proves to be beneficial.

The baseband transconductor is biased using an *nFET* based current-mirror. Each transconductor stage (a diff-pair) draws 21 mA of *dc* current. Ideally, a current-mirror designed using SiGe HBTs would have been preferred, since the 1/f noise in HBTs is intrinsically orders-of-magnitude lower than the noise in nFET devices [12]. However, between the positive rail (V_{CC} = 5 V), and negative rail (ground), sufficient headroom is not available to operate a SiGe HBT based current-mirror; headroom of approximately

0.5 V was available for the current mirror to operate under. While this value works for room-temperature circuit operation, it would be problematic at lower temperatures. As the temperature decreases, the turn-on V_{BE} of all SiGe HBTs between V_{CC} and ground increases [12]. Thus at lower temperatures, the SiGe HBT would have been operating under hard-saturation, which would have worsened the overall performance of the quadrature modulator. Thus, reliable over-temperature performance won over lower 1/f noise issues, and an *nFET* current-mirror was employed.

3. *Commutator*

After the transconductor stage, the baseband signal travels up to the LO port, also known as the commutator. The commutator is driven with a continuous sinusoidal wave of the modulating signal's (LO) frequency. The LO is generated on-chip using a VCO. The design of the VCO is outside the scope of this chapter. Physically, the LO signal can be considered as the "entry-gate" of the mixer. Whenever the LO is applied, the mixer is turned ON; for small/zero LO signals, the mixer is considered to be OFF. At the output of the commutator, the mixing products are generated. At this stage, the mixing products are summed and fed to a load (resistor, balun, buffer, or amplifier). It is crucial that this stage is only influenced by the LO frequency, and not the BB tones or generated RF tones. For this reason, a very good port-to-port isolation is required in this design. As a general rule of thumb, the LO signal should be +20 dB higher than the BB/RF signal for the case of an upconverting/downconverting mixer.

4. Variable Gain Amplifier

For the IQ modulator being discussed, the outputs of the commutator stage were presented to a variable gain amplifier (VGA). The VGA serves the dual purpose of boosting the conversion-gain, while also providing a second degree of gain-control for the upconverted RF terms using digital circuitry (the first degree of gain control is achieved by the switchable resistors in the transconductor stage). The digital circuitry to

tune the VGA gain is outside the scope of this chapter. A conventional diff-pair topology was chosen for the integrated RF VGAs [109].

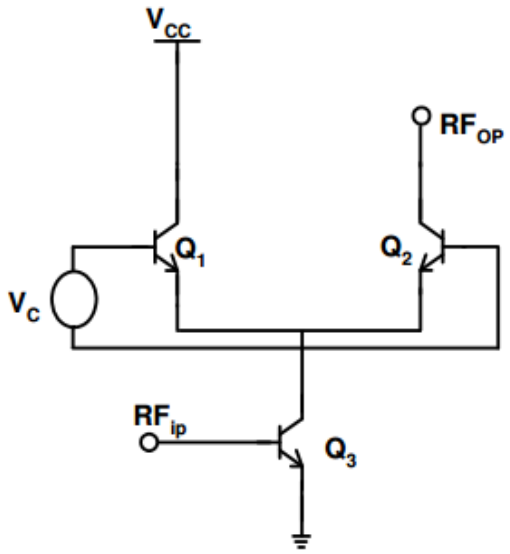

Figure 80: Conventional Gain-Control circuit.

In simple terms, the VGA can be thought of as a dual-cascode where two separate paths are available. In the first path, shown by transistor Q1 in Figure 80, the transistor Q1 steers the current and shunts it to the supply V_{CC} (which is an *ac* ground). In the second path, shown by transistor Q2 in Figure 80, the transistors steer the current (the signal component of which, as a reminder, was generated using the transconductor) to the RF output port. Control voltage V_C is applied differentially to base terminals of current steering devices for gain variation.

In the modulator design, gain-control using V_C as a tuning knob is applied to reduce the VGA gain for cases when the VGA output may risk compressing the input of the following stage. Four levels of gain control were provided, each reducing the conversion gain by 1-dB. In summary, to control the conversion gain of the modulator, the users have two tuning knobs at their disposal – changing the gain-control voltage within the VGA and changing the degeneration resistance values within the transconductor. Doing this will naturally affect the overall output linearity too.

5.4 Circuit: Simulation Results

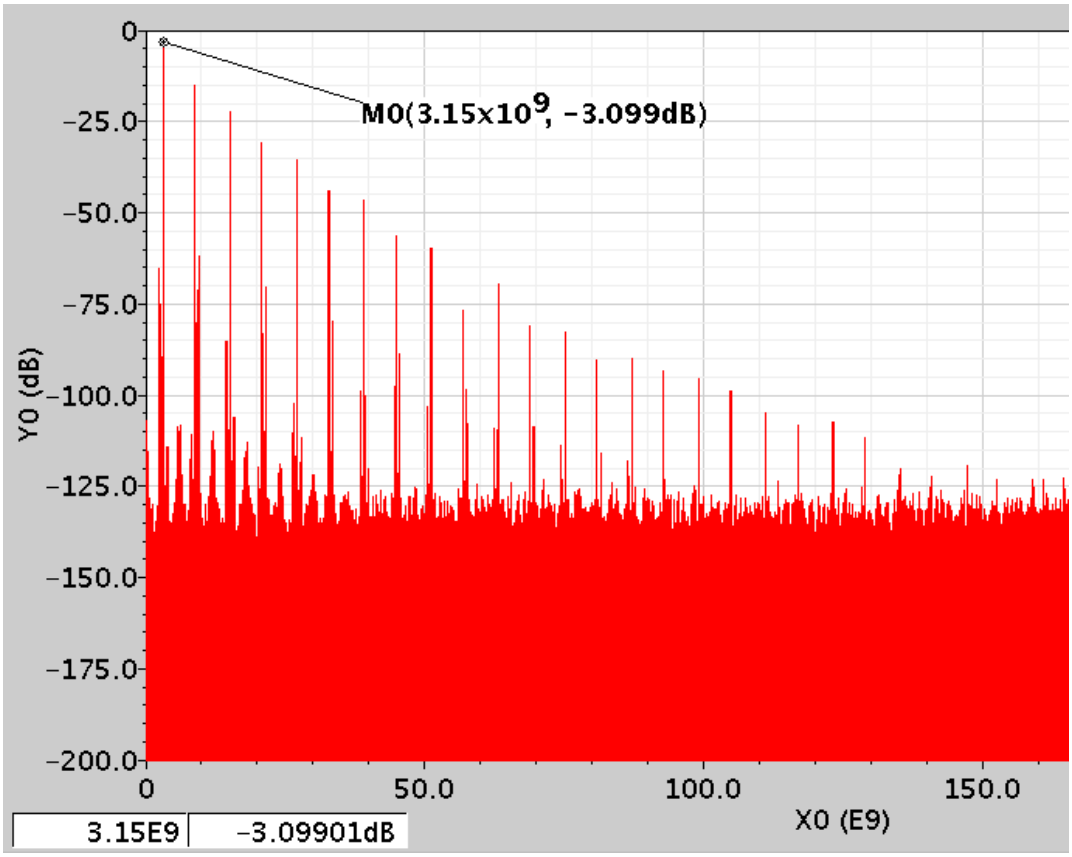

Figure 81: Spectrum of the output mixing tones.

Figure 81 shows the simulated output spectrum of the mixer. The baseband tones used in the simulation are 150 MHz and 200 MHz A common-mode baseband voltage was set to 0.25 V, which, performance-wise, is the more restrictive condition for the operation of the IQ modulator. For an input LO amplitude of 350 mV and baseband amplitude of 50 mV, the output power of the mixer at tones 3.15 GHz and 3.2 GHz is roughly -3 dBm. The load resistance in this case is 150 Ω, as that is the source impedance for the amplifier stage following the IQ modulator. Since this is a single-sideband double balanced mixer, it can be seen that neither the LO tones nor the two BB frequencies are present at the output. In addition, only the mixing products of 3.15 GHz and 3.2 GHz are generated at the output. The other two unwanted mixing products, 2.85 GHz and 2.8

GHz, are suppressed by more than -90 dBc relative to the desired mixing products in simulation.

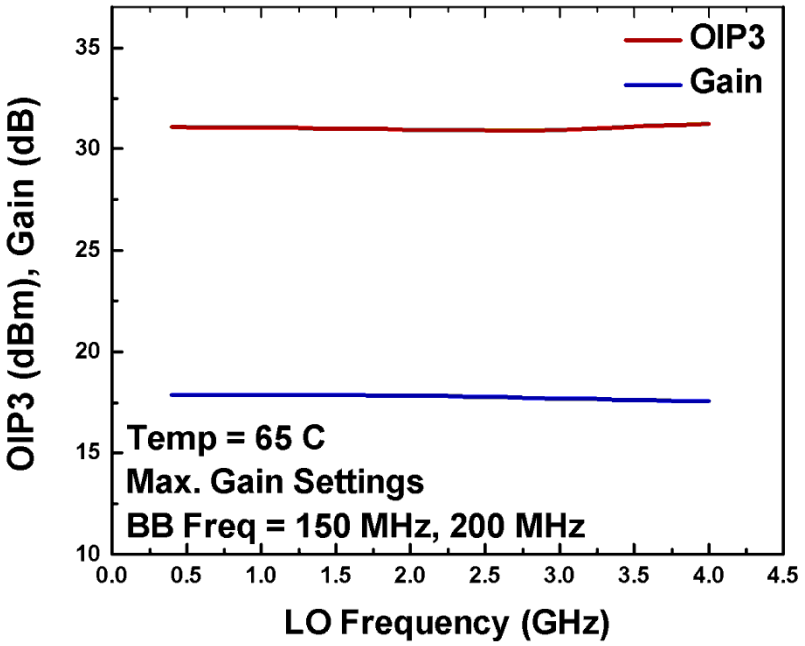

Figure 82: OIP3 and Gain as a function of swept LO frequency.

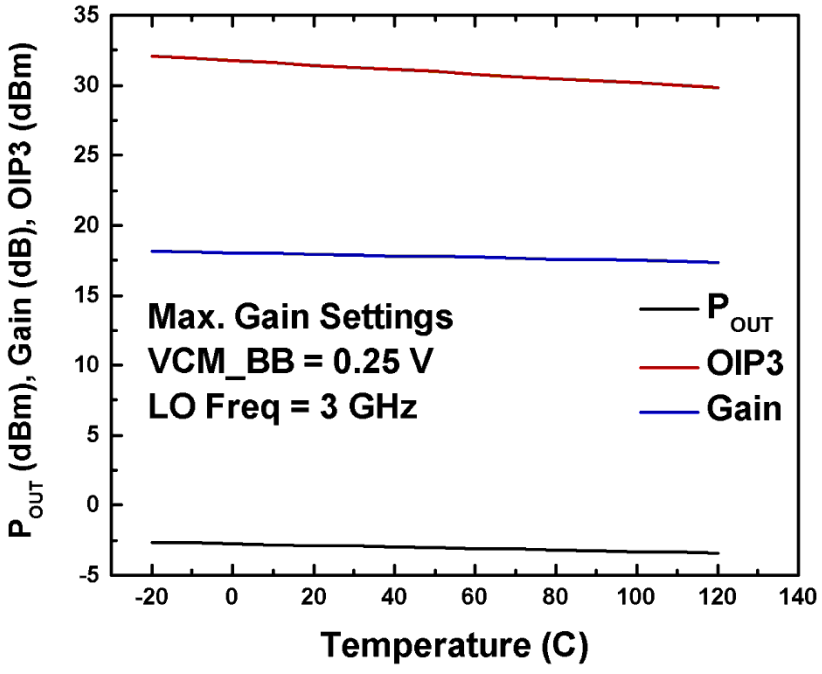

Figure 83: OIP3, Gain, P_{OUT} as a function of swept temperature.

Figure 82 shows the gain and OIP3 as a function of the swept LO frequency. It can be seen that the IQ modulator has a very flat gain across frequencies from 0.4 GHz to 4 GHz, as well as OIP3 always greater than +30 dBm. The temperature used for simulation was 65 C, to account for the heating of the package due to large currents flowing through the structure. For this simulation, all gain settings were set to provide maximum modulator gain.

Figure 83 shows the gain, OIP3 and output power of the IQ modulator with temperature varying from -20 C to 120 C. The OIP3 of the modulator improves slightly at lower temperatures. Overall, the circuit is very invariant to temperature. This was made possible in part by using FET-based current-mirrors instead of those based on HBTs. As mentioned previously, at lower temperatures, the turn-on V_{BE} of all the HBTs increases, thus leaving very little to no headroom for a HBT-based current mirror to operate effectively at reduced temperatures!

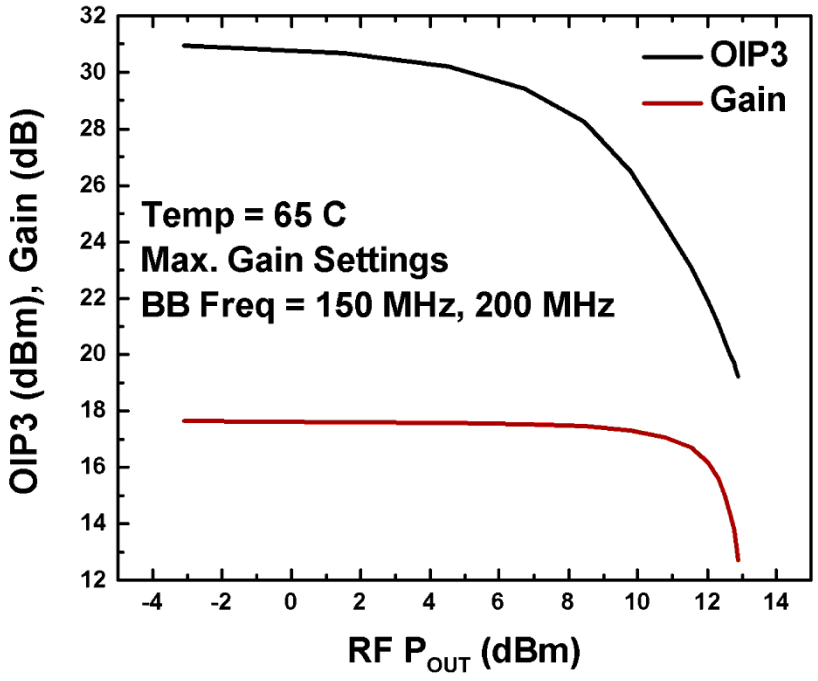

Figure 84: OIP3, Gain as function of P_{OUT}, to show gain compression.

Figure 84 shows the gain and OIP3 of the IQ modulator as they vary with output RF power. It can be seen that the output P1dB of the modulator is greater than 12 dBm (at the RF port). The tuning knobs for linearity are the gain settings in both VGA and transconductor, the *dc* current draw through the modulator chain, and the size of the transconductor core.

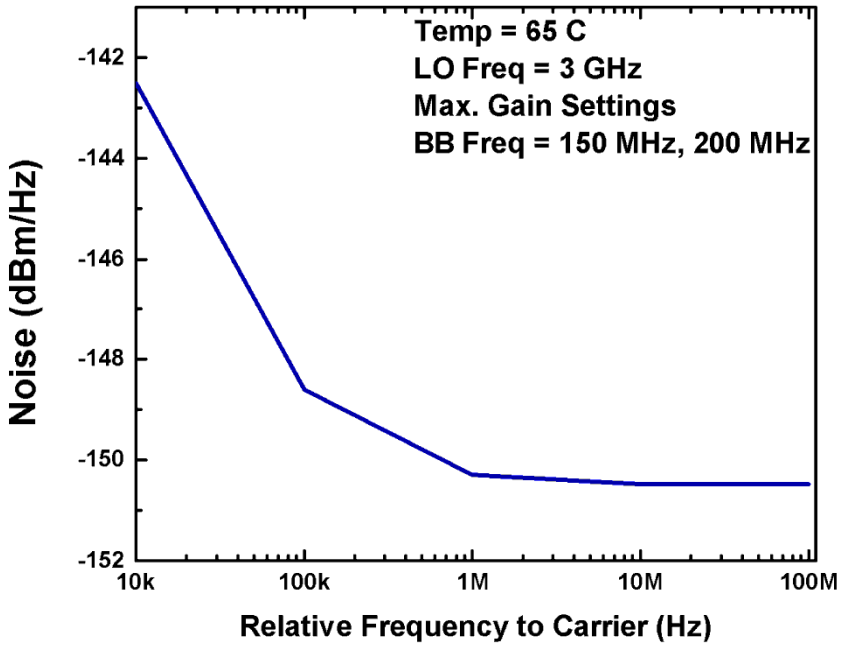

Figure 85: Noise analysis of the mixer.

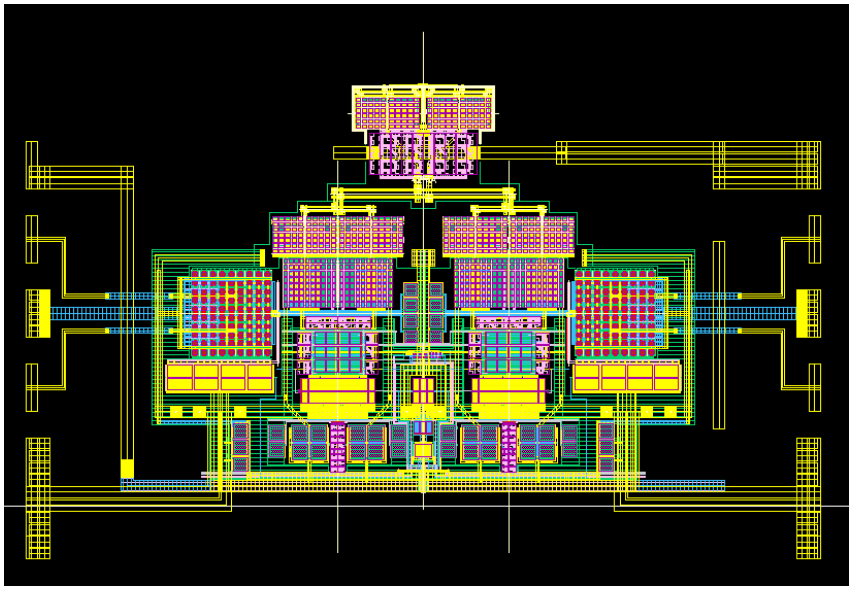

Figure 86: Layout of the IQ Modulator.

Figure 85 shows the output noise-floor of the IQ modulator. At 10 MHz offset from the carrier, the noise was simulated to be -150.4 dBm/Hz. This is a worst-case value, assuming an ambient temperature of 65 C. The tuning knobs to control noise are *dc* bias current through the HBTs, as well as the input resistance of primarily the transconductor stage. Figure 86 shows the layout of the IQ modulator. The pins padded out are either inputs from previous stages (LO, polyphase, digital circuitry), or an output to the amplifier.

5.5 Summary

In this section, the design of a SiGe-based high-linearity IQ modulator was presented. Starting at the device level, a comprehensive and systematic selection of the HBT geometry to maximize the OIP3 of the modulator was performed. The IQ modulator is currently under fabrication, and measurements results are expected imminently. A table highlighting the mixer performance is shown below.

Table 4: Performance metrics of the SiGe IQ modulator.

RF Output frequency range	0.4 – 4 GHz
Conversion Gain	17.7 dB
Output P1dB	12.1 dBm
Output IP3	+30 dBm
Noise Floor	-150.4 dBm/Hz at 10MHz offset
DC power consumption	400 mW

CHAPTER VI

CONCLUSION AND FUTURE WORK

6.1 Summary of Contributions

This dissertation explores the performance limits that can be achieved by complementary (*npn* + *pnp*) SiGe HBTs for designing high-performance RF front-ends. Amongst other things, the enhancement of dynamic range in RF front-ends was given special attention. As a part of this comprehensive study, device level metrics such as linearity and reliability were analyzed and the outcomes of those analyses were applied to the design of high-performance circuits such as RF switches, X-Band LNA, and cellular-band IQ modulator. The contributions of this research are summarized as follows:

1. A comprehensive analysis of transistor-level linearity for *npn* and *pnp* SiGe HBTs. It was found, for the first time ever, that *pnp* SiGe HBTs have a higher linearity than conventionally used electrically-matched *npn* HBTs. This result paves the way for high-performance complementary or *pnp*-only RF circuit design. Rigorous mathematical analysis based in Volterra Series was used for the first time to understand the underlying mechanisms behind the differences in linearity for the two types of HBTs.
2. A comprehensive analysis of the transistor-level reliability under extremely high-power RF stresses. This novel study lead to the conclusion that *pnp* SiGe HBTs are intrinsically more robust under damaging RF power levels than their electrically-matched *npn* counterparts. This is a crucial result for the design of highly robust and reliable complementary (or *pnp*-only) RF front-ends.
3. A comparison of two competing compact models for SiGe HBTs, the VBIC and the HICUM, to evaluate their ability to simulate intermodulation distortion in RF circuits with a high degree of accuracy. For the first time, it was found that the HICUM model is a better choice for predicting not only small-signal linearities

such as IIP3, but also large-signal distortion metrics such as gain compression. This result helps the semiconductor foundries to focus their efforts on developing only one compact model for HBTs; it also establishes the compact model of choice for high-fidelity RF circuit design.

4. A new methodology to extend the dynamic range of SiGe-based RF switches. Using the SiGe HBTs in the inverse-mode of operation delays the onset of compression in RF switches. A framework to easily analyze these results was presented, and guidelines for the design of a SiGe HBT with inherently high linearity characteristics for use in RF switches were established.
5. A new methodology to mitigate crosstalk in mixed-signal circuits across cryogenic temperatures. Techniques such as concentric rings of Deep Trenches, as well as increasing the physical separation between the noise-injector and sensor were analyzed both experimentally and analytically over cryogenic temperatures. It was found that the crosstalk increases drastically with reducing temperatures. This work has immediate implications for designers of mixed-signal circuits for extreme environment applications.
6. A method to use SiGe HBTs in low-power, high-performance RF front-end design by using the HBTs in the weak-saturation region of operation. It was found that even under drastically reduced voltage rails, the SiGe HBTs had very aggressive RF performance metrics, paving the way for SiGe-based ultra-low-voltage RF circuit design.
7. Design and analysis of a low-power and low-voltage X-Band SiGe LNA. The LNA was designed using two stages of common-emitter HBTs, which were operating under weak-saturation (WS) regime. Because of this, the LNA consumes only 2.4 mW *dc* power and has a gain of 17 dB. This yields a gain per *dc* power consumption FOM of 6.95 dB/mW. This is by far the highest reported FOM to-date for SiGe X-band LNAs.

8. Design of a highly linear cellular-band upconversion IQ modulator. A Gilbert Cell topology was employed to implement an upconverting double-balanced mixer. The chip is under fabrication. The RF frequency output range is 0.4 – 4 GHz. The simulated OIP3 of the mixer is greater than +30 dBm. The conversion gain is almost 17 dB. The output P1dB is 12.1 dBm. The simulated noise floor, at 10 MHz offset, is -150.4 dBm/Hz. The chip is invariant in performance from -20 C to 120 C. To our knowledge, these are currently the most aggressive specs compared to other commercially available upconverting IQ modulators.

6.2 Future Work

Based on the research presented in this thesis, several excellent opportunities for future work can (and should!) be considered. These areas of study are summarized here:

1. It has been repeatedly demonstrated in this dissertation that the *pnp* SiGe HBTs are superior in RF performance than electrically-matched *npn* SiGe HBTs in a complementary process. This result is still not widely known in the RF design community. To enhance these results further, an apples-to-apples comparison of a *pnp*-only and *npn*-only RF circuit (such as an LNA) would be very helpful. With a comprehensive performance comparison (NF, IIP3, Gain etc) at a circuit level, the superiority of *pnp* SiGe HBTs for use in RF design can be easily established.
2. Investigating the distortion performance of *npn* and *pnp* SiGe HBTs at cryogenic temperatures. It was established a few years ago that cryogenic distortion characteristics are a very strong function of HBT collector design. Since the collector in *pnp* SiGe HBT is doped much higher than *npn* HBTs, this would lead to very different linearity results at cryogenic temperatures. Such a study would not only be the first of its kind, it would also lead to the discovery of hitherto unknown novel device physics.

3. Developing faster *pnp* SiGe HBTs in TCAD. The f_T and f_{MAX} of *npn* SiGe HBTs is reaching near-terahertz speeds. Due to their superior RF performance, the *pnp* SiGe HBTs can play a crucial role in high-performance millimeter wave front-end design. Thus, immediate efforts need to be expended to make faster *pnp* SiGe HBTs in a complementary BiCMOS process.
4. Developing an HBT (*npn* or *pnp*) in TCAD with the express aim of enhancing its dynamic range. In this thesis, several means of enhancing dynamic range at the device level were discussed. Using techniques such as variable collector doping, germanium profile tailoring, and deployment of evenly-spaced Deep Trenches, the inherent dynamic range of SiGe HBT can be vastly improved.
5. Investigating the role that ionizing radiation plays on the weak-saturation (WS) regime of a SiGe HBT. There is good reason to believe that performance in the WS regime will degrade to a larger degree, compared to the forward-active mode, when exposed to damaging radiation. Performance degradation in WS regime under radiation has never been quantified and is crucial to completing the feasibility study of weakly-saturated circuits in space-based applications.
6. Improving the performance of the first-pass circuits presented. For example, the WS LNA presented in this work had inductor layout issues, which degraded the noise-matching at the input. With improved inductor layout, the Noise Figure of the WS LNA can be brought down to sub-2 dB domains. For the high dynamic range RF switch design, HBT geometries were not optimized for minimizing insertion loss. These design fixes can vastly improve the performance of the circuits presented.
7. Admittedly a challenging task, but designing a full receive-only chain in SiGe with a supply voltage of less than 1 V. Work presented in this thesis establishes the feasibility of this task. Demonstrating it would lead to record-performance receiver design!

APPENDIX A

MATLAB CODE

A.1 Intermodulation Calculation Using Volterra Series

The inputs to this code are:

1. Swept V_{BE} values at a fixed V_{CE} value (can easily be extended to do nested V_{CE} sweeps)
2. Corresponding base and collector *dc*-currents associated with voltage sweep in step 1, as well as calculated transconductance g_m.
3. Extracted C_{BC} and C_{BE} values from S-parameter simulations at frequency of interest, as well as transit-time tau (τ) for every *dc*-bias point using method described in [37].

```
% Beginning of file 'CalculateIIP3.m'
% Master file to calculate IIP3 for a given value of dc-bias conditions and extracted
%capacitances, after the CMNA method described in [36] and [12].

load npnHBT_Vce2volts_inputstoVolterracode.mat;

%%
%This file contains all the dc currents and extracted transconductance and capacitances for the
%HBT. Each parameters from this file can also be individually loaded into the program.


%Define circuit Passives like Load and Source Terminations
Rseries=50;
Rload=50;

%Reading inputs from the *.mat file loaded in line 1
Ic = Collector_current_from_file
Ib = Base_current_from_file
CBC = Cbc_column_from_file
CBE = Cbe_column_from_file
BETA = Ic./Ib;
taumatrix = tau_from_file   %Transit time calculated from S-parameters
Vcb = Vce.-Vbe_list_from_file;

f1=9.5E9;                   % Centre frequency in Hz
```

```
f2=f1;
tone_spacing = 1E6;                    % Tone spacing in Hz
f3=-(f1 + tone_spacing);

GM   = gm_column_from_file
K2GM = getK2GM(GM,Vbe);
K3GM = getK3GM(K2GM,Vbe);

K2cbcdepm = getK2GM(CBC,Vcb);
K3cbcdepm  = getK3GM(K2cbcdepm,Vcb);

K2cbedepm    = getK2GM(CBE,Vbe);
K3cbedepm = getK3GM(K2cbedepm,Vbe);

K2gmgbe=0;
K32gmgbe=0;
K3gm2gbe=0;
```

%%It always helps to smoothen all the derivatives to get smoother IIP3 results

```
for i=1:1:length(K3GM)
   Icmatrix(i)=Ic(i);                  %Defining the Ic matrix with length same as K3GMm; used in
PLOT in the end
   beta = BETA(i);

   tau = taumatrix (i);
   gm = GM(i);
   gbe = gm/beta;
   K2gm = K2GM(i);
   K2gbe = K2gm/beta;
   K3gm = K3GM(i);
   K3gbe = K3gm/beta;

   Cbe = CBE(i);
   Cbc = CBC(i);

   K2cbediff = 0;                                  %Or can also try tau*K2gm;
   K2Cbe = K2cbediff+K2cbedepm(i) ;                %Total K2c value for the Cbe capacitor


   K2cbcdep = K2cbcdepm(i);
   K2Cbc = K2cbcdep;                               %Total K2c value for the Cbc capacitor

   K3cbediff = 0;                                  %Or can try tau*K3gm;
   K3Cbe = K3cbediff+K3cbedepm(i);


   K3cbcdep =  K3cbcdepm(i);
   K3Cbc = K3cbcdep;                               % Total K3c value for the Cbc cap

   H1f1 = h1calc(Rseries,Cbe,Cbc,Rload,gm,gbe,f1);          %Calculates H1 matrix for f1
   H1f2 = h1calc(Rseries,Cbe,Cbc,Rload,gm,gbe,f2);          %Calculates H1 matrix for f2
   H1f3 = h1calc(Rseries,Cbe,Cbc,Rload,gm,gbe,f3);          %Calculates H1 matrix for f3
```

```
        H2f1f2 =
        h2calc(Rseries,Cbe,Cbc,Rload,gm,gbe,f1,f2,K2gbe,K2gm,K2Cbe,K2Cbc,K2gmgbe);
%Calculates H2 matrix for f1,f2
        H2f2f3 =
        h2calc(Rseries,Cbe,Cbc,Rload,gm,gbe,f2,f3,K2gbe,K2gm,K2Cbe,K2Cbc,K2gmgbe);
%Calculates H2 matrix for f2,f3
        H2f1f3 =
        h2calc(Rseries,Cbe,Cbc,Rload,gm,gbe,f1,f3,K2gbe,K2gm,K2Cbe,K2Cbc,K2gmgbe);
%Calculates H2 matrix for f1,f3


        inl3gbe = K3gbe*H1f1(1)*H1f2(1)*H1f3(1) + .66*K2gbe*(H1f1(1)*H2f2f3(1) +
        H1f2(1)*H2f1f3(1) + H1f3(1)*H2f1f2(1));

        inl3gm  = K3gm*H1f1(1)*H1f2(1)*H1f3(1)  + .66*K2gm*(H1f1(1)*H2f2f3(1) +
        H1f2(1)*H2f1f3(1) + H1f3(1)*H2f1f2(1));

        inl3c1 = j*2*pi*(f1+f2+f3)*K3Cbe*H1f1(1)*H1f2(1)*H1f3(1) +
        j*2*pi*0.66*(f1+f2+f3)*K2Cbe*[H1f1(1)*H2f2f3(1) + H1f2(1)*H2f1f3(1) +
        H1f3(1)*H2f1f2(1)];

%C1 is the Cbe capacitor

        inl3c2 = j*2*pi*(f1+f2+f3)*K3Cbc*[H1f1(2)-H1f1(1)]*[H1f2(2)-H1f2(1)]*[H1f3(2)-H1f3(1)] +
        j*2*pi*0.66*(f1+f2+f3)*K2Cbc*[(H1f1(2)-H1f1(1))*(H2f2f3(2)-H2f2f3(1)) + (H1f2(2)-
        H1f2(1))*(H2f1f3(2)-H2f1f3(1)) + (H1f3(2)-H1f3(1))*(H2f1f2(2)-H2f1f2(1))];

%C2 is the Cbc capacitor

%avalanche current term calculation\

        inl3t1 = 0.33*K2gmgbe*[H1f2(1)*H2f1f3(2) + H1f1(1)*H2f2f3(2) + H1f3(1)*H2f1f2(2) +
H1f2(2)*H2f1f3(1) + H1f1(2)*H2f2f3(1) + H1f3(2)*H2f1f2(1)];

        inl3t2 = 0.33*K32gmgbe*[H1f1(1)*H1f2(1)*H1f3(2) + H1f1(1)*H1f3(1)*H1f2(2) +
H1f2(1)*H1f3(1)*H1f1(2)];

        inl3t3 = 0.33*K3gm2gbe*[H1f1(1)*H1f2(2)*H1f3(2) + H1f1(1)*H1f3(2)*H1f2(2) +
H1f2(1)*H1f3(2)*H1f1(2)];

        inl3avl =  inl3t1 + inl3t2 + inl3t3 + inl3gm + inl3gbe;
%I usually end up putting this value as zero.

        Y3 = ycalc(Rseries,Cbe,Cbc,Rload,(f1+f2+f3),gm,gbe);
        H3 = inv(Y3)*[(inl3c2-inl3gbe-inl3c1);(-inl3c2-inl3gm)];
        IIP = abs(H1f1(2))/(Rseries*abs(H3(2)));
        IIP3(i) = 10*log10(1000*IIP);

end
```

% End of file 'CalculateIIP3.m'

% Beginning of file 'H1calc.m'

```
% H1 matrix calculations
```

```
function Hfinal = h1calc(Rseries,Cbe,Cbc,Rload,gm,gbe,f1)

        Y = ycalc(Rseries,Cbe,Cbc,Rload,f1,gm,gbe);
        Ys = 1/(Rseries);
% Temp variable created just to solve the equation 8.62 on page 342 Blue book

        Hfinal = inv(Y)*[Ys;0];
```

% End of file 'H1calc.m'

% Beginning of file 'H2calc.m'

```
% H2 matrix calculations

function Hfinal2 =
          h2calc(Rseries,Cbe,Cbc,Rload,gm,gbe,f1,f2,K2gbe,K2gm,K2Cbe,K2Cbc,K2gmgbe)

          H1f1 = h1calc(Rseries,Cbe,Cbc,Rload,gm,gbe,f1);
          H1f2 = h1calc(Rseries,Cbe,Cbc,Rload,gm,gbe,f2);
          inl2gbe = K2gbe*H1f1(1)*H1f2(1);
          inl2gm  = K2gm*H1f1(1)*H1f2(1);
          inl2c1 = j*2*pi*K2Cbe*(f1+f2)*H1f1(1)*H1f2(1);
%C1 is the Cbe capacitor
          inl2c2 = j*2*pi*K2Cbc*(f1+f2)*(H1f1(2)-H1f1(1))*(H1f2(2)-H1f2(1));
%C2 is the Cbc capacitor
          inl2avl =  0;%inl2gbe + inl2gm + .5*K2gmgbe*[H1f1(1)*H1f2(2) + H1f1(2)*H1f2(1)] ;
          Y = ycalc(Rseries,Cbe,Cbc,Rload,(f1+f2),gm,gbe);
          Hfinal2 = inv(Y)*[(inl2c2-inl2gbe-inl2c1);(-inl2c2-inl2gm)];
```

% End of file 'H2calc.m'

% Beginning of file 'ycalc.m'

```
% Y-matrix calculations

          function Yfinal = ycalc(Rseries,Cbe,Cbc,Rload,f1,gm,gbe)

          Ys = 1/(Rseries);
          Yl = 1/(Rload);
          A = i*2*pi*f1*Cbe;          %Temp variable for sCbe
          B = i*2*pi*f1*Cbc ;         %Temp variable for sCbc + depletion cap
          Yfinal = [(Ys+gbe+A+B) -(B);(gm-B) (Yl+B)];
```

% End of file 'ycalc.m'

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